SEMICONDUCTOR & ADVANCED PACKAGING NEWS

36 **Advanced Packaging | PCB / IC-Substrate – Reducing the environmental impact**
Gernot Schulz & Christof Wernbacher, AT&S & Roland Rettenmeier, Evatec

40 **Advanced Packaging | CLUSTERLINE® 600 & next generation IC-substrates**
Roland Rettenmeier

44 **Advanced Packaging | Cross-Contamination in Multi-Chamber PVD Systems**
Kay Viehweger, Fraunhofer IZM-ASSID & Dr. Patrick Carazzetti, Evatec

52 **Advanced Packaging | HEXAGON – Optimum R_c Control & productivity**
Kay Viehweger, Fraunhofer IZM-ASSID & Dr. Carl Drechsel, Dr. Patrick Carazzetti, Carl Wang, Dr. Juergen Weichart & Ewald Strolz, Evatec

58 **Power Devices | Frontside Processes – Trench filling & Planarization**
Fabian Kramer & Mohamed Elghazzali

62 **Power Devices | Power ICs: New Cu Frontside processes on 300mm**
Mohamed Elghazzali

64 **Power Devices | Investigating GaN sputter from a liquid Ga target**
Dr. Philipp Doering, Fraunhofer Institute for Applied Solid State Physics (IAF) & Thomas Tschirky, Evatec

68 **Power Devices | HEXAGON – double up in power device applications**
Fabian Kramer & Gerald Feistritzer

20 ANNIVERSARY

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AT EVATEC

Reducing the environmental impact in the PCB / IC-Substrate industry

AT&S experts ***Gernot Schulz*** and ***Christof Wernbacher*** togther with Evatec's ***Roland Rettenmeier*** explain how the CO_2 footprint of PCB manufacturing can be reduced by reducing raw materials and wet processes, optimizing product build ups and introducing dry processes.

AT&S – Playing its part

The Electronics industry as well as the PCB industry are undergoing a massive change in manufacturing. Governments, OEMs and customers all require a reduction of the CO_2 footprint and a resource-efficient use of raw materials, support materials, energy and water throughout the entire value/supply chain. The "Green Deal" is the European Union's response to this major global challenge for the future. Manufacturing companies are among the key players in the environmentally friendly economic development of tomorrow and are called upon to contribute to solving these challenges with their ideas and innovations. Various measures are available for this purpose: Switching to renewable energy, climate-friendly mobility, resource-conserving value chains, material innovations and intelligent product developments that are designed entirely for recycling.

Product Carbon Footprint – Wet chemical processes are the main contributor

The production process of printed circuit boards generally consisting of mainly wet chemical processes such as etching, galvanic or cleaning. Figure 1 gives an overview on how different production processes from classic PCB production contribute to the overall Product Carbon Footprint of PCB (PCF). Therefore, a sample product consisting of a 10-layer PCB with PTH and Laser Drills manufactured in AT&S production facility in HTB was chosen for this study. Several Energy and Chemical consumptions along the production chain were measured and broken down on product level. The contribution of the different process steps is highly dependent on PCB design such as number of layer, complexity and advanced technologies used. In general a significant amount of emissions are related to the energy and chemical intensive galvanic and etching process steps. Both are standard processes within the PCB production landscape and form the basis of a subtractive manufacturing approach. Since sustainability is in addition to costs and technology becoming a further focus point, additive manufacturing approaches which do not rely on wet chemical processes are becoming of greater interest.

One important part and door opener into additive manufacturing is the sputtering / PVD process. On one hand it improves PCB manufacturing from a technology point of view, on the other hand it allows us to reduce the amount of subtractive production processes.

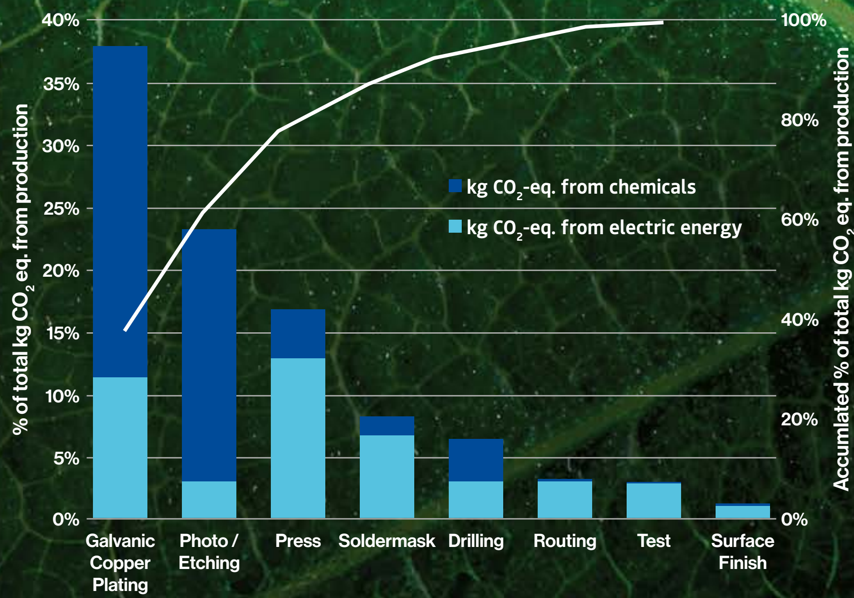


Figure 1: Carbon Footprint of different production processes

Novel technologies as a key to more sustainable products

To further substantiate this correlation, a study was initiated which allowed direct comparison of the environmental footprint between a PCB produced with Sputtering/PVD processes on Evatec's CLUSTERLINE® 600 versus a PCB produced with standard technology. This study was done as part of AT&S' initiative to better understand the environmental impact of different technology platforms and process groups. Therefore, the boundaries of the study were set around processes dedicated to a specific technology. The focus of the study was so called embedding technology, which allows the embedding of ICs as well as active and passive components directly into the PCB which gives numerous advantages especially from a technological point of view. Different technology levels are available with Center Core Embedding (CCE) being the current standard technology. The more sophisticated technology which is currently under development uses a Sputtering/PVD process.

For the comparison the main process steps of both technologies were quantified regarding their consumption of energy, chemicals, process gas and water. The environmental impact of the different input streams was assessed with a combination of primary data from material and energy supplier as well as data from ecoinvent database.

Figure 2 shows the comparison of the Carbon footprint between both technologies. The new generation embedding technology shows a significant reduction, mainly due to a reduction of energy and chemical consumption. This reduction can be achieved because of the more efficient product design becoming feasible with new technology. The process gas which is only used in the new generation embedding technology does not have a serious impact on the overall result.

As an additional benefit, which is not considered in the assessment, the new generation embedding technology also increases the utilization of the panel according to the die to package ratio, which basically indicates how densly the Integrated Circuits (IC) can be placed onto the Package. Considering this improvement, the advantage of the new technology is even more significant.

In addition to embedding technology, Sputtering/PVD processing has the potential to increase the opportunities in PCB design not only in terms of technological aspects, but also in terms of more sustainable design. Different Life Cycle Assessments of PCBs have shown that reducing layer counts as well as reducing the size of a single PCB for better utilization of the production panel leads in most cases to a significant improvement of the Product Carbon footprint.

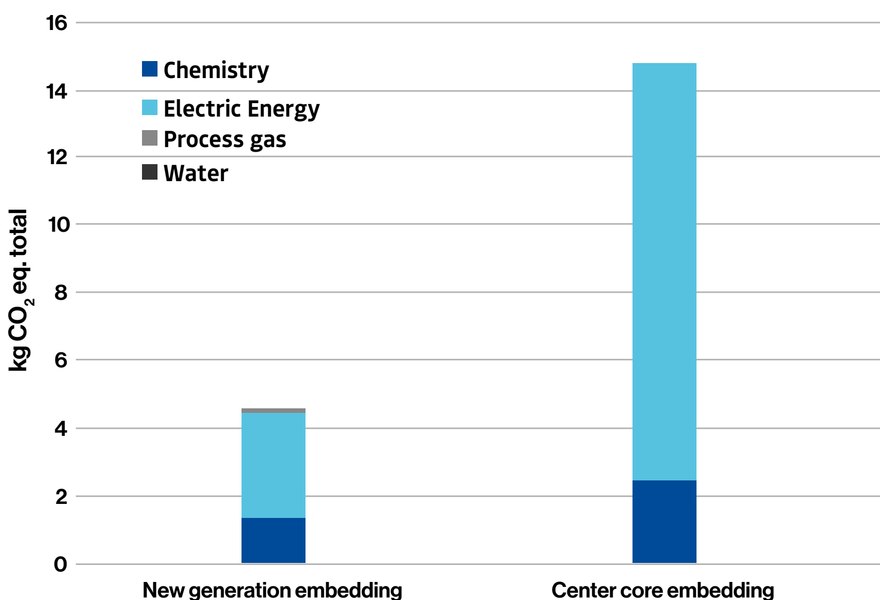


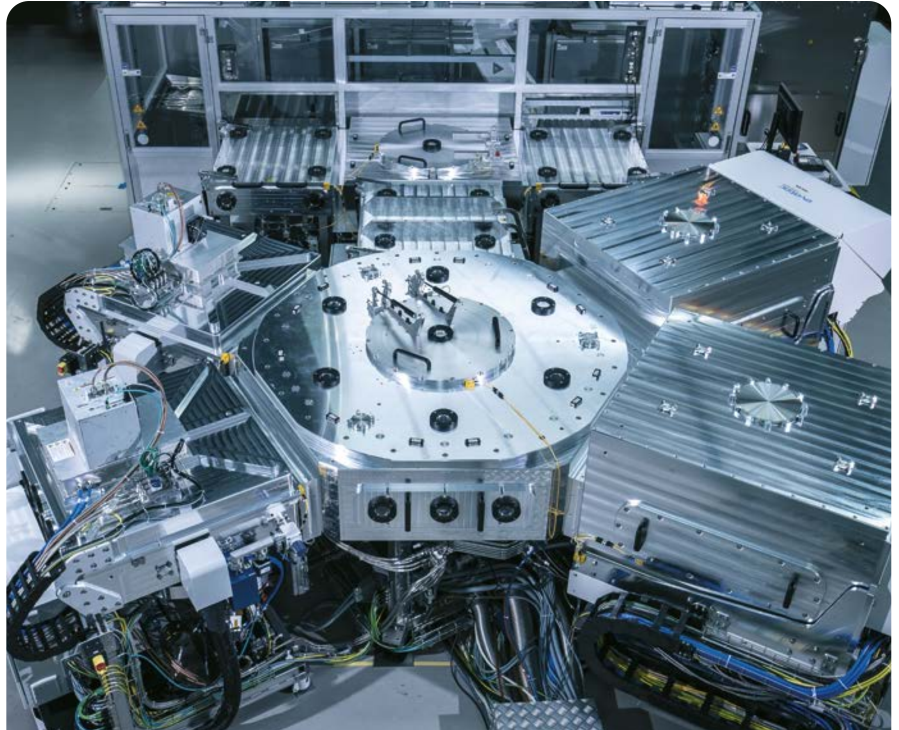
Figure 2: Carbon Footprint of new generation embedding technology compared to standard embedding technology

Improvement beyond carbon footprint

The focus of the industry and branch in Europe is definitely on reduction of the carbon footprint due to the several large initiatives such as the EU Green Deal or the Paris Agreement which are focusing on Greenhouse gas reduction. But to gain a holistic picture of environmental impact it is also necessary to take a look on further influences (for example environmental impact categories according to CML-2016). For all these categories beyond the carbon footprint AT&S plans to extend these assessments to create a more complete picture. But especially for PVD/Sputtering process and the opportunities coming with this technology an even larger improvement is expected than for the carbon footprint, since the reduction of wet chemical processes and therefore chemistry usage is highly connected to other benefits e.g. reduction human toxic substances, acidification potential or nutrification potential. Due to the fact that Sputtering/PVD is also considered as one key technology for miniaturization of electronic components such as PCB or IC Substrates, it can also make its contribution to reducing the global e-waste problem. With miniaturization approaches the relative amount of e-waste can be reduced by simply reducing the volume and mass of the electronic components. Overall more dry process steps in PCB production will lead to less impact on the environment from the industry sector.

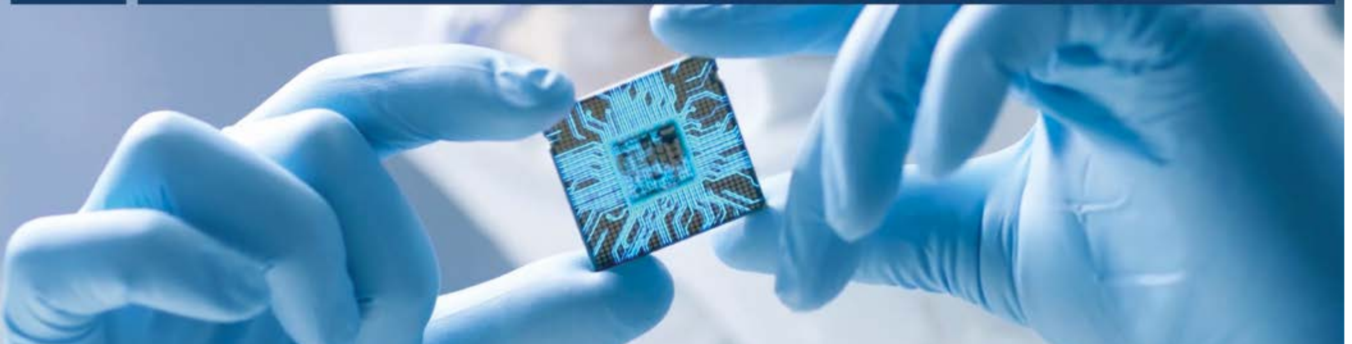
Heading in the right direction

The PCB industry has been trying to find novel technologies and processes to reduce the amount of wet chemical subtractive processes within the manufacturing landscape since many years. The internal and external pressure to reduce the environmental footprint of PCB production is now bringing an additional argument to go in this direction. Sputtering/PVD process technology now seems to be the most promising approach. Direct comparison with conventional technology shows a significant improvement from both sides – ecologically and technologically. Currently the technology is used for special use high end cases, but when it finds its way to more commodity use cases also high volume applications can profit from the environmental impact reducing processes.



CLUSTERLINE® 600

To read about Evatec's CLUSTERLINE® 600 sputter platform and some of the most recent technological developments go to page 40 or visit **evatecnet.com/products/clusterline-family/clusterline-600**



A view of AT&S*

Technology and digitalization are having an ever-growing impact on our lives and are increasingly shaping our daily routines at home and at work. The advances achieved in these fields in recent years are truly breathtaking and have created crucial momentum for growth in every sector of the economy. As a global technology enterprise, AT&S is actively involved in these developments and plays a decisive role in shaping the digital world of tomorrow. This also represents an enormous responsibility, which AT&S has always accepted and fulfilled through its forward-looking vision, pioneering investments in research and development, and responsible use of resources. The high-end PCBs and IC substrates AT&S supplies influence future industry standards, products and applications in a number of key industries.

Want to know more? Visit **https://ats.net/en/** or complete the contact form at **https://ats.net/en/contact/**

**Source: AT&S website*

CLUSTERLINE® 600 Perfect for next generation IC-substrates too!

The potential benefits of moving from wafer to panel processing including much higher material and process utilization are already well documented (Figure 1). Evatec's Senior Product Marketing Manager ***Roland Rettenmeier*** takes us through some of the recent developments on the well established CLUSTERLINE® 600 platform. These updates in capability make it the perfect choice for customers when setting up manufacturing capability for emerging markets like advanced IC-substrates for applications such as Artificial Intelligence, and other High Performance Computing applications.

Evatec Collaborates with Onto Innovation in Panel Level Packaging Applications Center of Excellence

To find out more about the co-operation read the article

Advanced Packaging Technologies for the future – Building on a common portfolio of process technologies

Evatec's CLUSTERLINE® 300, CLUSTERLINE® 600 and HEXAGON, feature the same process concept for Advanced Packaging:

- Atmospheric batch degas for preparing substrates with organic load for best in class vacuum processing
- ICP or CCP Etch technology (with arctic cooling) for highly uniform etch prior to deposition
- Long life PVD sources for lowest cost of ownership in high volume manufacturing

CLUSTERLINE® 600 – A proven pedigree in high volume manufacturing

Evatec's CLUSTERLINE® 600 panel processing tool was built leveraging the know-how gained across Evatec's wafer level processing platforms over many years and has already established itself as the market leading system for panel processing. Built around a central Vacuum Transfer Module (VTM), the tool can be equipped with up to 5 single process modules (SPM) for etch or deposition. An atmospheric front end module (AFEM) handles substrates in and out of FOUPS stationed on up to 6 Load Ports (LP). Pre-processing via Evatec's unique Atmospheric Batch Degasser (ABD) followed by two stage pumping brings substrates into vacuum in perfect condition for any etch and deposition processes. A typical configuration is shown in Figure 2.

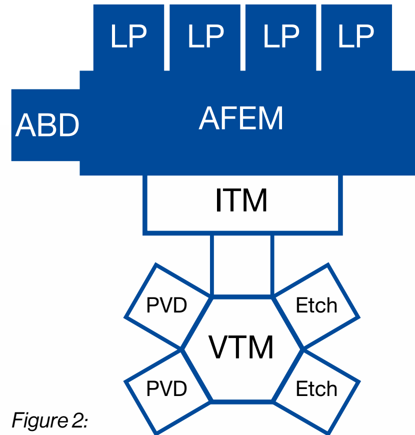
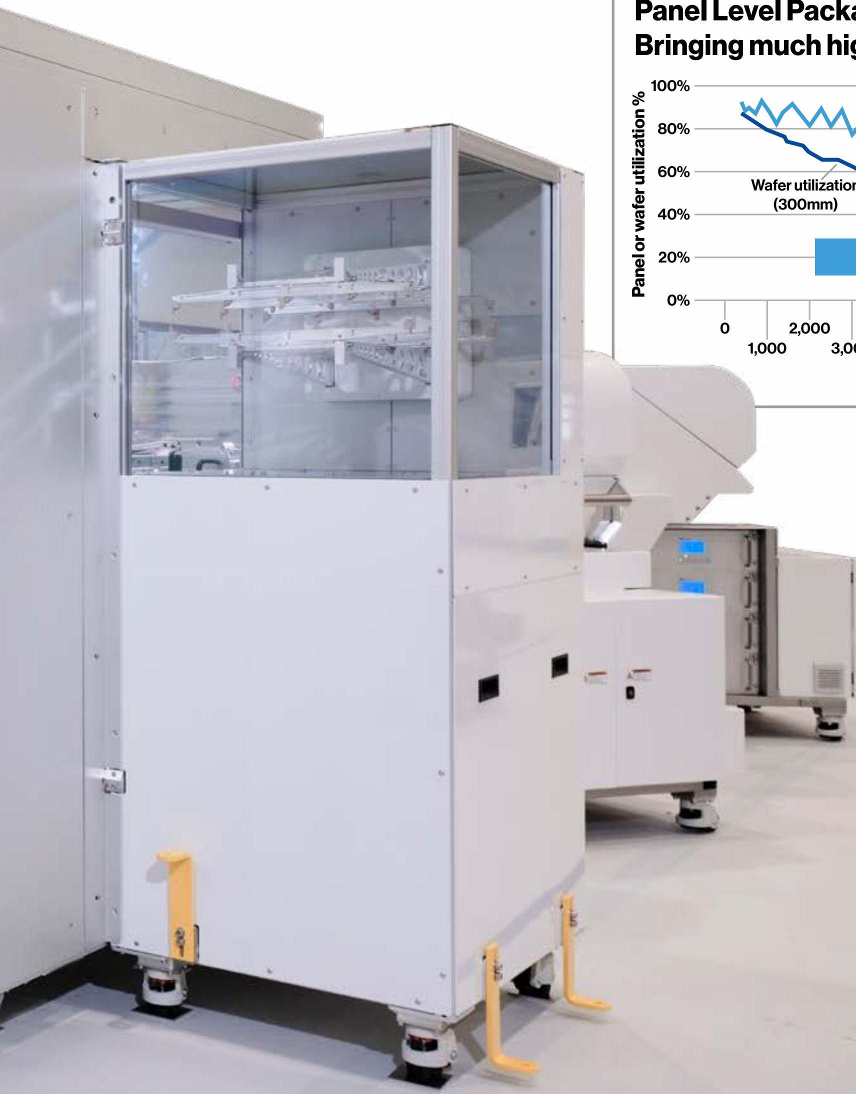


Figure 2:

By the start of 2024 there were more than 10 CLUSTERLINE® 600 working in volume manufacturing around the world. The latest developments on the tool make it ready to handle next generation IC-substrates.



Panel Level Packaging – Bringing much higher material and process utilization

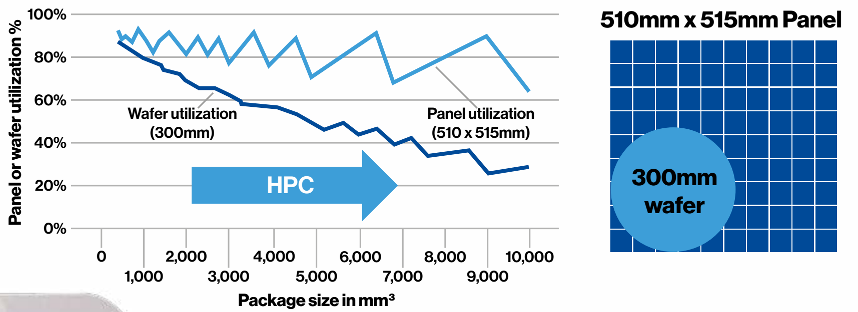
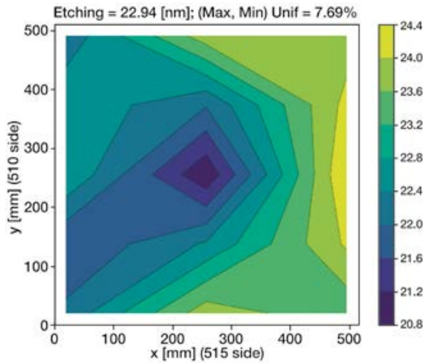
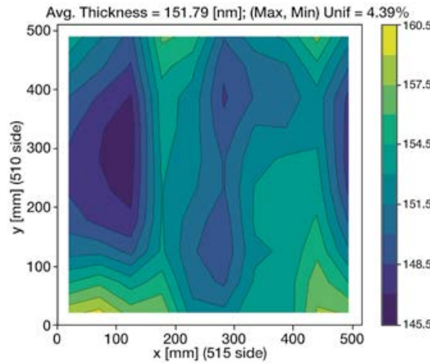


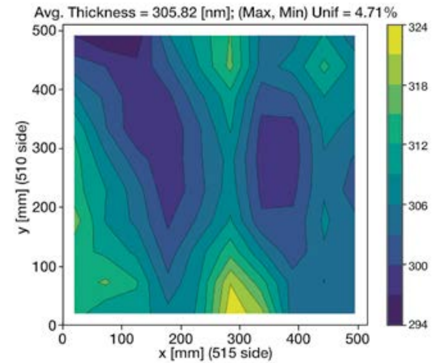
Figure 1:

Some typical process results

Low contact resistance (R_c), excellent adhesion and low particles are paramount. Typical process performance results of etch and deposition processes for Ti and Cu are shown below.







Etch

Etching uniformity better than 10%, for etching amount of 20nm (SiO_2 equivalent), with etch rate higher than 0.15nm/s.

Ti deposition

Thickness uniformity better than 6% for 150nm Ti deposition. Sputter rate higher than 100nm/min and Rs ≤ 75 uOhms*cm.

Cu deposition

Thickness uniformity better than 6% for 300nm Cu deposition. Sputter rate higher than 200nm/min and Rs ≤ 3.5 uOhms*cm.

New tool features now available

Ready for advanced substrates

Newly designed end effectors for handling thin substrates down to 100µm thickness and recessed chucks with full "Keep Out Zone" (KOZ) functionality ensure that active areas are not touched during handling and processing.

High performance robust handling – flipping

The latest AFEM design can accomodate up to 6 Load Ports and features a substrate flipper for double sided processing.

A view from Yole Group

The Glass era starts in the advanced IC substrate and semiconductor equipment industries.

The advanced packaging industry is at a new inflection point with the arrival of glass as a new core material. Announced by Intel in September 2023, this next generation of Advanced IC substrates will be adopted to overcome the limitations of organic core substrates and easily meet the demands of high-performance computing (HPC) and AI trends, opening new options such as flexible form factors and better mechanical stability.

Glass, as a material, offers superior dimensional stability, thermal conductivity, and electrical properties compared to the built-up organic substrates. However, glass introduces challenges in handling and processing, requiring precise care during manufacturing. Additionally, inspection and metrology processes for glass substrates necessitate specialized equipment to ensure quality and reliability.

Despite these challenges, the adoption of glass core substrates is driven by the demand for larger substrates and the technological trend toward chiplets and heterogeneous integration.

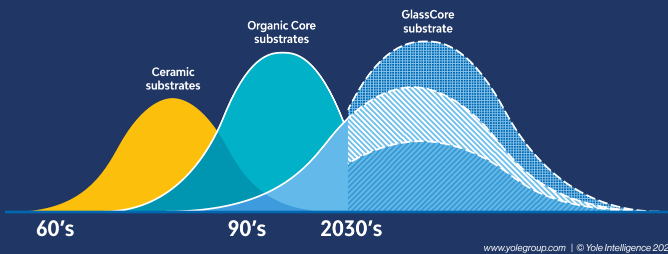
Within this landscape, Through Glass Via (TGV) technology is crucial, facilitating higher connection density and superior signal integrity for high-speed circuits. While TGVs offer performance benefits, they also present manufacturing challenges and higher production costs. Recent advancements in TGV-related patents are aiding the commercialization of glass core substrates.

The synergy between glass core substrates, organic core substrates, and panel-level packaging (PLP) is driving the adoption of panel-adapted equipment by offering enhanced chip density, reducing costs, and improving manufacturing efficiency and yield. As GCS technology matures, it promises to redefine the advanced packaging landscape, particularly for AI accelerators and servers, paving the way for next-generation chip designs and packages.

The increasing growth of AI and its next-generation AI accelerators is driving a significant increase in chip package sizes. Current AI accelerators typically have package sizes around 70 to 80 mm. However, the growing need for larger packages, exceeding the limits of organic substrates at 120 by 120 mm, presents a challenge to the advanced packaging industry. To address this demand and offer a cost-effective solution, the industry is shifting towards panel utilization and related equipment, enabling the production of larger chip packages at reduced costs.

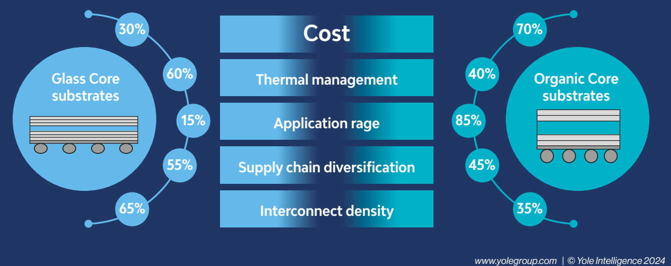
Market adoption trends of Glass Core Substrates

Source: Satus of the Advanced IC Substrate Industry report, Yole Intelligence, 2023



Advanced IC Substrate – comparison with Organic Substrate material

Source: Satus of the Advanced IC Substrate Industry report, Yole Intelligence, 2023



About the author

Bilal Hachemi, Ph.D., is a Technology & Market Analyst, Semiconductor Packaging at Yole Group.

Working within the Manufacturing & Global Supply Chain activities at Yole Group, Bilal contributes daily to the analysis of packaging technologies, their related materials, and manufacturing processes.

Previously, Bilal carried out experimental research in the field of nanoelectronics and nanotechnologies, focusing on emerging dielectric materials and their ferroelectric applications. He (co-) authored several papers in high-impact scientific journals and participated in several international conferences.

Bilal obtained a Ph.D. in nanoelectronics in 2022 from the Grenoble Alpes University (France), and he studied at IAE Grenoble for a management master's degree.

Study of Cross-Contamination in Multi-Chamber PVD Systems Used for High-Throughput Seed Layer Deposition

Modern WLP application require PVD systems that can deliver low and stable contact resistance (R_c) at high throughput. HEXAGON is an excellent candidate to fulfill this role. This study demonstrates that chamber-to-chamber cross-talk during continuous run is negligible compared to the residual outgassing of the etched wafer itself as explained by ***Kay Viehweger*** from Fraunhofer IZM-ASSID, Germany, and Evatec's Senior Process Engineer, ***Dr. Patrick Carazzetti***.

Abstract

Higher interconnect density in WLP applications increases the importance of interconnect quality, measured by contact resistance (R_c). UBM and RDL metallization are key steps. HEXAGON shows 50% lower Rc and 40% higher throughput than the CLUSTERLINE®. Cross-contamination mainly comes from residual outgassing of etched PBO wafers.

Introduction

Wafer-level packaging (WLP) technologies play a key role in supporting the continuous miniaturization, increased functionality and better power efficiency required by the ever more sophisticated system-on-chip (SoC) and system-in-package (SiP) architectures [1,2]. The downscaling of the critical design dimension and the concomitant increase of I/O density per unit area, has increased the need for a tighter control of the contact resistance (R_c). R_c is referred as the ohmic resistance between the uppermost level of the active circuitry and the metal routing to the bumps. In fact, R_c is directly related to the performance of the packaged device, such as the overall power consumption and signal integrity [3-5]. High-volume manufacturing (HVM) relies on magnetron sputtering for the deposition of adhesion/seed layers that are necessary for the subsequent formation of under bump metallization (UBM) and redistribution layers (RDL). The sputtered PVD stack primarily provides the adhesion function to the underlying pad and organic dielectric passivation, and also a conductive layer for electroplating. Prior to the sputter deposition, state-of-the-art multi-chamber PVD systems perform dedicated pre-treatment steps to improve the metal adhesion to the dielectric. First, the degas step drives out moisture from the dielectric film, which is especially necessary for hydrophilic organic materials, such as Polyimide (PI) or Polybenzoxazole (PBO) [6-8]. This is to avoid that excessive water molecules re-emerge during the subsequent fabrication steps. Secondly, the wafer is sputter cleaned using a mild Argon plasma bombardment to remove oxides from the metal contacts (usually Al or Cu pads) formed through the organic passivation. This etch clean, is typically an inductively-coupled plasma (ICP) process operating at low bias voltage (<600 volts) to avoid device damage. Next, without breaking vacuum, the wafer undergoes the sequential deposition of the Ti-adhesion and Cu-seed layers. The load of organic volatile byproducts generated during the non-selective Ar sputter etching must be efficiently removed from the system to avoid contamination of the other process stations. Since the final device performance is measured only upon completion of the entire WLP process, it is critically important to manage the contamination level and to ensure that especially the Ti-adhesion layer capping the I/O contacts, is deposited in a clean environment that prevents oxide re-growth and contamination from hydrocarbon species.

Previous research presented a benchmark of throughput and R_c performance of two competing PVD systems architectures used in the manufacturing of UBM and RDL metallization. These PVD systems are the HEXAGON and the CLUSTERLINE®, respectively. Data generated in wafer-level chip-scale packaging (WLCSP) have demonstrated that the HEXAGON can consistently deliver 50% lower R_c baseline for a corresponding 40% higher throughput [9]. Further hardware developments of the HEXAGON platform were done to boost its handling speed. This improvement has demonstrated that the HEXAGON can maintain low and constant R_c values even at record throughput of 80.0 wafers/hour [10]. Beside the overall better performance obtained on the HEXAGON compared to the CLUSTERLINE®, there is an aspect of the former platform that has not been sufficiently investigated. In fact, the indexing concept itself, based on the simultaneous transfer of all wafers, would make this platform critically exposed to cross-talk between the different process stations. This can result in an excessive contamination of the PVD chambers, primarily due to the load of organic volatiles species propagating from the ICP sputter etch chambers. The consequence could be the contamination of the metal interfaces, which may adversely impact the R_c of the fabricated device.

This work presents a side-by-side comparison of the cross-contamination dynamics occurring in the HEXAGON and CLUSTERLINE® PVD systems employed in their current HVM

configuration. Residual Gas Analysis (RGA) is used to characterize the level of contamination in two strategically important locations of both platforms. These are the vacuum transport module (VTM) and the Ti deposition chamber.

Hardware Characteristics and Process Strategies

The main hardware characteristics, process strategies and performance of the two platforms are compared in Table I. More than a decade ago, the "arctic" ICP etch chamber was introduced to tackle new process challenges arising from the poorly vacuum compatible organic passivation materials, which were starting to see widespread use as dielectric layers in WLCSP applications [9]. The concept basically consisted in actively cooling the process environment by means of an external chiller unit supplying coolant fluid to the pedestal and the chamber shields.

Essential Hardware Characteristics, Process Strategies and Performance of the PVD Platforms Presented

The chilled pedestal coupled with Argon back-gas provides in-situ cooling to the substrate during process. Whereas the active cooling of the metal shields counterbalances the heating effect induced by the plasma process, thereby mitigating additional outgassing from the organic material residues already present in the chamber. In addition to the active cooling, the pumping efficiency of the chamber was also improved. Furthermore, aluminium pasting was introduced as a periodic conditioning procedure to keep R_c low and stable and to extend the shields lifetime [11]. The Atmospheric Batch Degas (ABD) was developed to deal with heavily outgassing substrates, such as the Epoxy-mold compound (EMC) used in Fan-Out wafer-level packaging (FOWLP) applications [9]. In the ABD, a batch of wafers is loaded into a heated metal cassette and exposed to a laminar flow of N2 for a minimum time of 20 minutes.

Several advantages inherent to its configuration, as well as the dedicated process strategies allow the HEXAGON platform to reach best-in-class R_c at higher throughput compared to the CLUSTERLINE®. Two aspects which are believed to play a key role are discussed hereafter. First, the faster chamber-to-chamber transfer time allows to minimize the time interval between the end of the ICP sputter etch and the beginning of the sputter deposition of the Ti-adhesion layer. This is believed to decrease the risks of recontamination or reoxidation of the cleaned contacts. Secondly, the strategy of splitting the ICP etch amount in two chambers is beneficial to contain the residual outgassing load in the first chamber, while the contact cleaning is completed in the second chamber relatively free from volatile contaminants.

Typically, a multi-chamber PVD system operates in a regime where the throughput limitation comes from the longest sequence executed in one of the process chambers. Steady-state operation mode is achieved when consecutive batch of wafers are processed in the system without interruptions. The residence time in the ABD does not represent the bottleneck as long as neither its capacity, nor the process time impact the regular flow of wafers to sustain continuous loading of the airlock. The handling speed of the platform comes into play during the chamber-to-chamber wafer transfer. From the R_c standpoint, it is therefore strategically important to setup the process flow in such a way to minimize the transfer time occurring between the end of the ICP sputter etch and the beginning of the Ti deposition. Practically, this is achieved by imposing the etch sequence to become the time bottleneck of the entire flow. In the case of the HEXAGON, where the etch amount is split over two chambers, the process sequence is programmed in such a way that the second chamber becomes the bottleneck.

Topic	Platform type	
	HEXAGON	CLUSTERLINE®
Transport in atmosphere	▪ Combined Gantry / SCARA 5-axis robot	▪ Combined Gantry / SCARA 5-axis robot
Transport in vacuum	▪ Central servo motor with revolving carousel	▪ Bisymmetric arm robot
Wafer transfer time in vacuum [sec]	▪ 13.0 (older generation) ▪ 8.0 (new generation)	▪ 28.0 – 30.0
Airlock cycle time [sec]	▪ 25.0-28.0 (single unit) ▪ Wafer capacity: 1	▪ 50.0-56-0 (2 units operating in parallel) ▪ Wafer capacity: 2
Pumping system (high vacuum)	▪ Airlock: turbo ▪ Process chambers: turbo ▪ VTM: turbo and cold traps	▪ Airlock: turbo ▪ ICP etch chamber: turbo ▪ PVD chambers: Cryo ▪ VTM: Cryo
Degas strategy	▪ Atmospheric Batch Degas (ABD) for WLCSP & FOWLP	▪ Single-wafer vacuum degas for WLCSP ▪ ABD for FOWLP
Cooling station	▪ Dedicated process chamber with chilled pedestal, wafer clamp and back-gas	▪ Not implemented
ICP sputter etch strategy ("arctic" chamber)	▪ Two serial etch chambers (50/50 split etch amount) ▪ Chilled pedestals and metal shields (-30°C)	▪ Single etch chamber ▪ Chilled pedestal and metal shields (-30°C)
Aluminium pasting strategy (ICP chamber)	▪ Automated by SW, with aluminum plates stored in atmospheric buffer station	▪ Automated by SW, with aluminum plates stored in atm. or vacuum buffer stations
Throughput [wafers/hour]	▪ 90-100 (handling limited) ▪ 45-55 (process limited[a])	▪ 40-45 (handling limited) ▪ 26-34 (process limiteda)
Rc [mΩ] (source OSATs)	▪ 7.0 ± 0.3 ▪ Al pasting frequency every 10 prod. wafers	▪ 7.5 - 12.0 ▪ increased Al pasting frequency

[a]Depending on the aluminium pasting frequency.

Thermal model

The typical process-of-records (POR) used in UBM/RDL production are reported in Figure 1 along with the simulated thermal profiles of a 300 mm Silicon wafer. Despite the tool configurations differ by the number of process chambers used, the process output in terms of (1) degas time and temperature, (2) etching amount and (3) PVD stack thickness remains the same. Based on the substrate properties, the thermal model calculates the heating rates of the different plasma processes involved, as well as the cooling rates during transfer and in-situ cooling provided by “arctic” etch and Ar backside gas. In the HEXAGON tool, the first process chamber in vacuum fulfills the role of cooling station. Here the substrate is mechanically clamped to the chilled pedestal for 50 sec. At the same time, Argon is applied at the wafer backside to increase the cooling efficiency. The combination of the cooling step and split etch approach results in a substrate temperature of 145°C (Figure 1a). On the other hand, the absence of the cooling station on the CLUSTERLINE® and the full etch amount performed in a single chamber result in a 40°C higher peak temperature (Figure 1b). In general, a lower temperature after the etching process is another beneficial aspect that helps to reduce outgassing and the related risk of recontamination, thus contributing to a better R_c control. The POR run on the HEXAGON results in a peak temperature of 170°C at a throughput of 54.5 wafers/hour. The CLUSTERLINE® POR reaches a peak temperature of 186°C and 33.3 wafers/hour throughput.

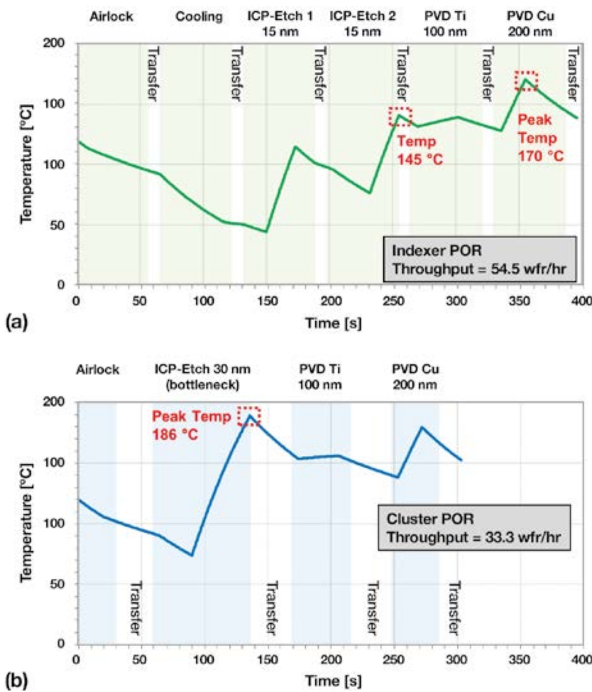


Figure 1a & 1b: Thermal profiles of a 300 mm Silicon wafer processed with UBM/RDL POR on the HEXAGON (a) and on the CLUSTERLINE® (b).

Wafer transfer in the HEXAGON

During process, the chamber pedestal is in the upper position and the cylindrical bellow fixated to the pedestal pushes the wafer carrier against the chamber flange. The isolation of the chamber is realized by compressing the two Viton seals inserted in the upper surfaces of the bellow and in the carrier against the above metal surfaces [12] (Figure 2 (a)). The transfer sequence is illustrated in Figure 2 (b)-(e). As soon as the bottleneck sequence is completed, the control SW issues the transfer command. The transfer sequence starts by the synchronized pneumatically driven down-stroke movement of all pedestals, which takes approximately 2.0 seconds. This action compresses the chamber bellows and consequently unseals the process environment in regard of the VTM. During the down movement, the wafers are placed on the carriers mounted on the HEXAGON carousel. The carousel plane is situated at an intermediate level between the two extreme positions of the pedestal. When the pedestals are in the lower position, the HEXAGON is free to move. At this moment, the servo motor drives in 3.0 sec the 60°-clockwise rotation of the carousel. As a result, all wafers are transferred simultaneously to the subsequent process station. It is important to note that during the indexing phase, process chambers and VTM share the same vacuum conditions. Next, the synchronized 2.0 sec up-stroke movement of the pedestals lifts the wafers from the carriers and seals again the chambers from the VTM. Now the wafers are sitting on the chuck top and the process sequence can start. In the new HEXAGON platform with central servo motor, the whole wafer transfer sequence takes approximately 8.0 sec. This is 5.0 sec faster compared to the earlier platform generation with a gear-driven carousel.

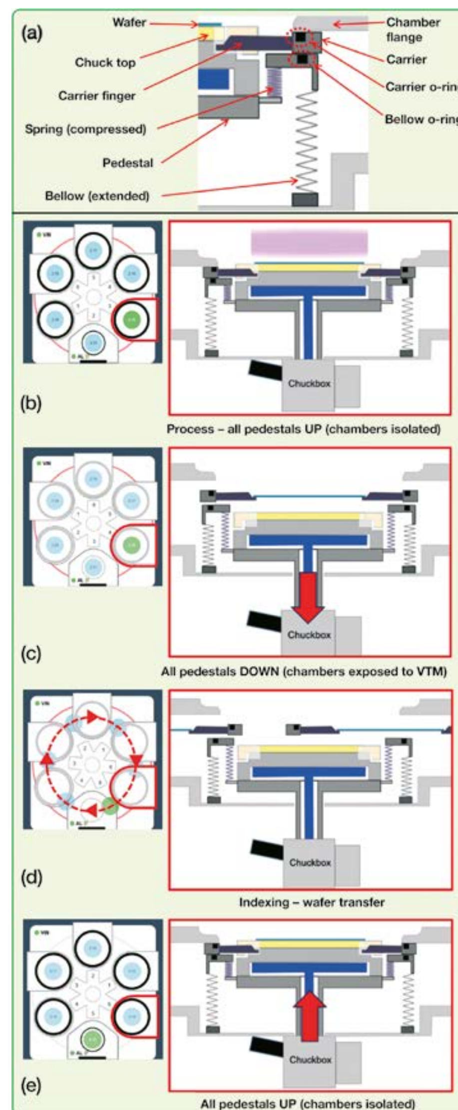


Figure 2: Chamber cross section (a) and wafer transport steps in the HEXAGON with central servo motor (b)-(e).

Wafer transfer in the CLUSTERLINE®

The transfer sequence in the CLUSTERLINE® is illustrated in Figure 3. Up to six process chambers and two airlock units are clustered around the VTM. The latter is equipped with a bisymmetric arm robot performing pick-&-place operation. All process stations and

airlocks are isolated from the VTM by means of individual slit valves. The valve opens prior wafer pick and closes after the next wafer has been placed. Thus, the VTM is exposed to the process chamber environment for a 15.0 sec time interval. The pedestal of the process chamber is actuated by a servo motor, and this is allowed to move only when the slit valve is closed. Both the down and up-stroke movements require approximately 10.0 sec. The total chamber-to-chamber transfer in the CLUSTERLINE® is approximately 30.0-35.0 sec. This corresponds also to the time interval between the end of the ICP sputter etch sequence (flow bottleneck) and the start of the Ti deposition. During steady-state operation, it can be observed that one wafer remains on standby on one of the robot arms until the ICP etch chamber becomes available (Figure 3 (a)). Since the wafer in question was previously degassed in the ABD, its temperature remains in the order of 100°C and thus continues to outgas and contaminate the VTM during its residence.

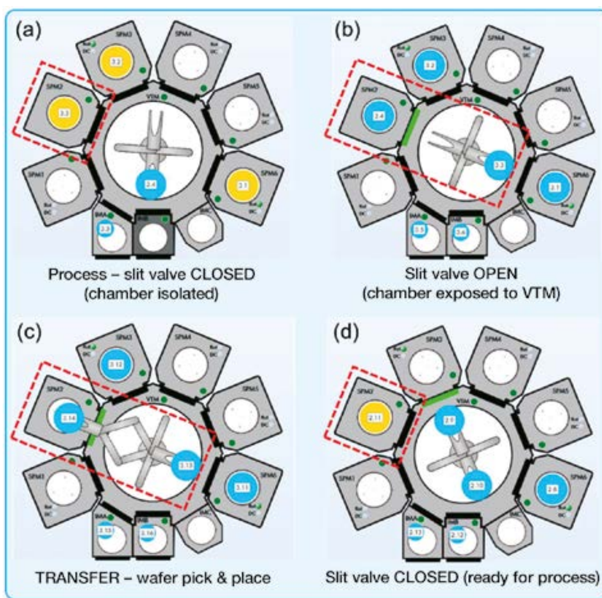


Figure 3: Wafer transport sequence in CLUSTERLINE® with bisymmetric-arm robot in the VTM. Each chamber is isolated from the VTM by means of individual slit valves.

Airlock cycle

Figure 4 compares the airlock performance of both systems. The pressure curves were recorded during a cycle run of SiO2 wafers. The pumpdown and venting time, as well as the wafer transfer time in vacuum and atmosphere are indicated. The reduced volume and the pumping scheme of the HEXAGON airlock are optimized for fast vent/pump cycle. Typically, the pumpdown time from atmosphere to the vacuum threshold 5.0E-5 Torr requires 10.0 sec. The venting time with N2 takes approximately 5.0 sec. During the movement of the airlock pedestal followed by the indexing, the pressure measured in the airlock is in the order of 1.0E-5 Torr, meaning two decades higher than the pressure of the VTM (not shown here). This different pressure level in regard of cross-contamination will be discussed in Section IV.

The control SW of the CLUSTERLINE® manages the operation of two airlock units in parallel. Each airlock has a capacity of two substrates. The upper position is reserved for the incoming substrates, which have been previously processed in the ABD. The lower position is reserved for the outcoming wafers, whose process is complete and are transferred back to the FOUP. The typical pumping time to the vacuum threshold of 5.0E-5 Torr is 25.0 sec and the venting time is 16.0 sec (Figure 4b). The slower pump and vent result in part from the larger airlock volume compared to the HEXAGON design. In the example shown, the base pressure of the airlock approaches 1.0E-5 Torr for a residence time of 40.0 sec. Then, as soon as the slit valve opens to allow the wafer transfer, the airlock pressure drops due to the lower pressure level of the VTM. During the indicated 14.0 sec necessary for placing the outgoing wafer and picking the incoming wafer, the VTM is to some extent exposed to the contamination from the residual atmosphere of the airlock.

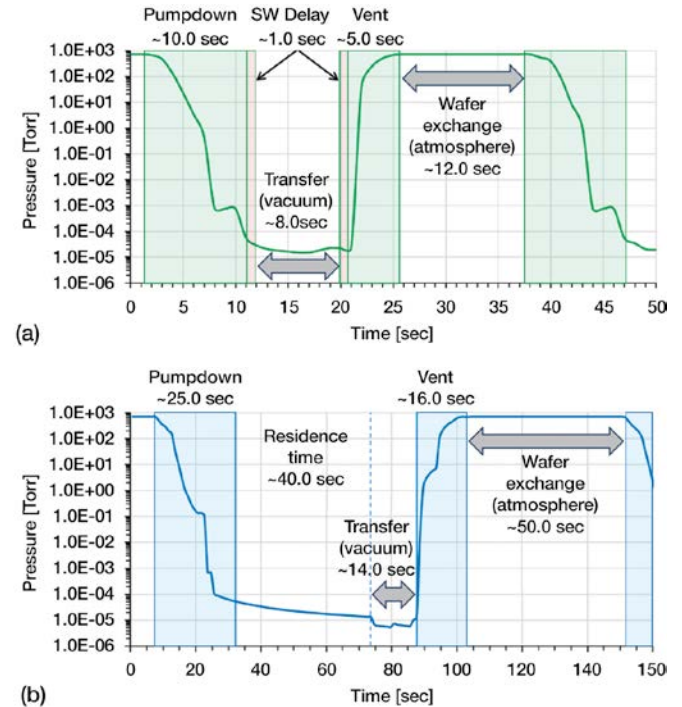


Figure 4a & 4b: Airlock pressure curves indicating pumping/ venting and transfer time: HEXAGON (a) and CLUSTERLINE® (b). In both cases SiO_2 wafers were used.

Experimental Method

A series of tests is conducted on 300 mm wafers to characterize the contamination caused by the residual outgassing. RGA measurements are performed with HPQ3 model from MKS, whose upper working limit is 1.0E-3 Torr [13]. RGA devices are installed in two strategically important locations of the PVD platforms, namely the VTM and the Ti deposition chamber. Measurement in the VTM provides information on the outgassing propagating from the process chambers during the time interval when the wafers are in transit. Whereas data collected in the PVD-Ti chamber provides information on the background contamination before the start of the film deposition. Two different sets of wafers were used to execute the test plan summarized in Table II. A batch of 25 Si wafers with 5'000 Å of thermal oxide grown on both frontside and backside was used as a reference of non-outgassing material. A second lot of 25 Si wafers coated with 9.0 µm of PBO was used to mimic the outgassing of real products with organic passivation. RGA data of both wafer lots are presented in Section IV.

Design of Experiment – Datasets Collection

Platform	RGA location	Wafer type (25-wafers run)	
HEXAGON	VTM	SiO_2	PBO
	PVD-Ti	SiO_2	PBO
CLUSTERLINE®	VTM	SiO_2	PBO
	PVD-Ti	SiO_2	PBO

Figure 5 illustrates the system configuration, the locations of the RGA and the corresponding flow used to process the test wafers. Degas and ICP sputter etch processes were performed according to the POR previously described. In contrast, no metal was sputtered in the PVD chambers, instead the wafers were kept in vacuum for 50.0 sec. The RGA spectra were recorded from 1 to 50 a.m.u. during continuous wafer run.

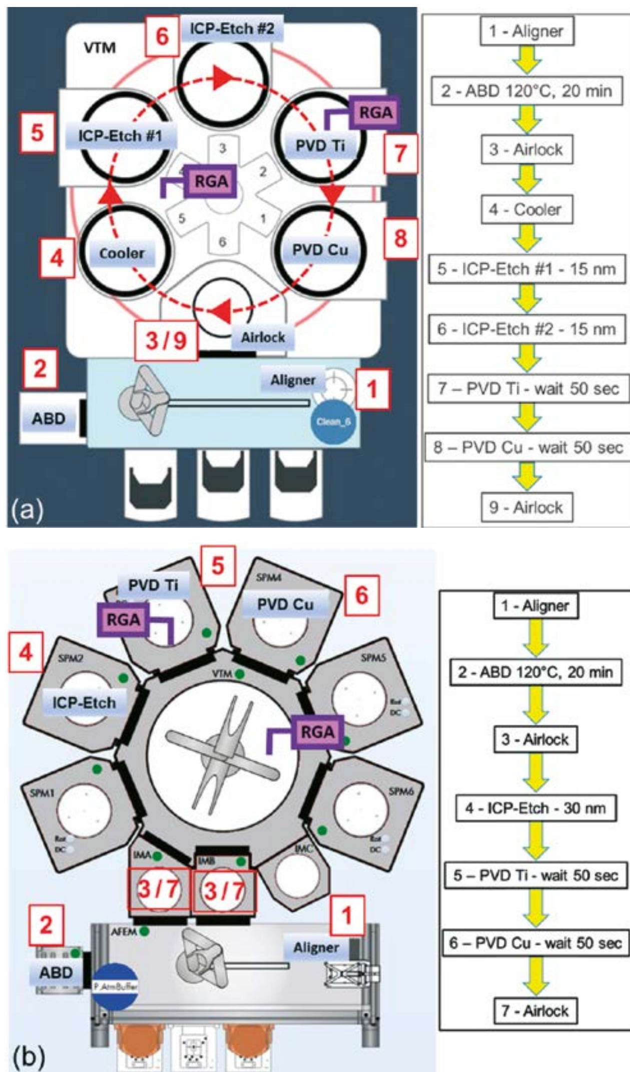


Figure 5: Configuration of the PVD systems used in HVM: HEXAGON (a) and CLUSTERLINE® (b). The process flows executed to run the cross-contamination tests are indicated beside each platform.

Results

Each dataset presented in the next paragraphs refers to a 25-wafers lot. To avoid a too clogged display, each chart is limited to a timespan of 300 sec, which is sufficient to describe accurately the behavior of the lot. The masses of the different species present in the spectra were identified based on available libraries [14]. The results are presented and discussed based on a selected group of the most prominent masses measured. These are in part originated from the Argon process gas, such as masses 40 and 20, which are attributed to Ar+ and Ar++. The other masses considered are related to the volatile contaminants. Masses 18, 17 and 16 can be attributed to the presence of water molecules (H2O+) and the corresponding fragments, i.e. HO+ and O+. However, mass 16 can also be related to the ion CH4+. The presence of organic contaminants is normally indicated by the species with mass 28 (CO+) and mass 44 (CO2+). The signal of mass 28 can also be attributed to nitrogen (N2+) as a specie present in the base pressure of the system and in the residual airlock atmosphere. Finally, mass 32, attributed to O2+, is also monitored.

HEXAGON – VTM RGA: SiO_2 vs. PBO Wafers

Figure 6 (a) and (b) displays the RGA spectra measured in the VTM of the HEXAGON during the process of SiO_2 and PBO wafers. The partial pressures of 4 known contaminants are compared in Table III. Masses 16 and 17 are omitted from the table as the former normally shows a marginal partial pressure and the second follows closely the trend of mass 18. Each of the pressure peaks, indicate that a transfer cycle takes place. At the instant t1 the pedestals move down to allow the rotation of the carousel. This event corresponds to a sharp increase of the VTM pressure. The contributors to this increase are: (1) the residual airlock atmosphere, (2) the residual Ar process gas, and (3) the volatile byproducts generated during the etching process. During transfer, at t > t1, the VTM pressure is mainly dominated by masses 40 and 20. In the case of PBO wafers, masses 28 and 40 are significantly more prominent than on SiO_2 wafers. This reflects the presence of byproducts generated during etching of this organic film. After transfer, the chambers are again isolated from the VTM environment. The pressure promptly recovers and stabilizes within seconds. At the instant t2 the Argon species practically disappear from the spectrum and the difference between the wafer types can be seen mainly by the higher partial pressure of masses 28 and 44. In both cases, at t3 the main contributors to the VTM pressure are masses 18 and 17.

The time interval between consecutive transfer events, e.g., t1 and t3, represents the wafer cycle time. When the cycle time is stable and constant, this can be used to calculate the steady-state throughput as indicated below:

Throughput = 3600/cycle time [wafers/hour] (1)

The HEXAGON is running the process outlined in Figure 5a operates at a cycle time of 65.5 sec, which corresponds to a steady-state throughput of 55.0 wafers/hour.

CLUSTERLINE® – VTM RGA: SiO_2 vs. PBO Wafers

Figure 7a and 7b compare the RGA spectra measured in the VTM of the CLUSTERLINE® during the process of SiO_2 and PBO wafers. The partial pressures of the contaminants are reported in Table IV. The steady-state regime is reached when the process stations used by a given process flow are fully populated. This means, for instance, that the transfer history exhibits a periodic behavior throughout the job. In the steady-state conditions reached in this test, the vacuum robot necessitates 52 sec to transfer one-by-one the 5 wafers present in the system at once. The sudden pressure

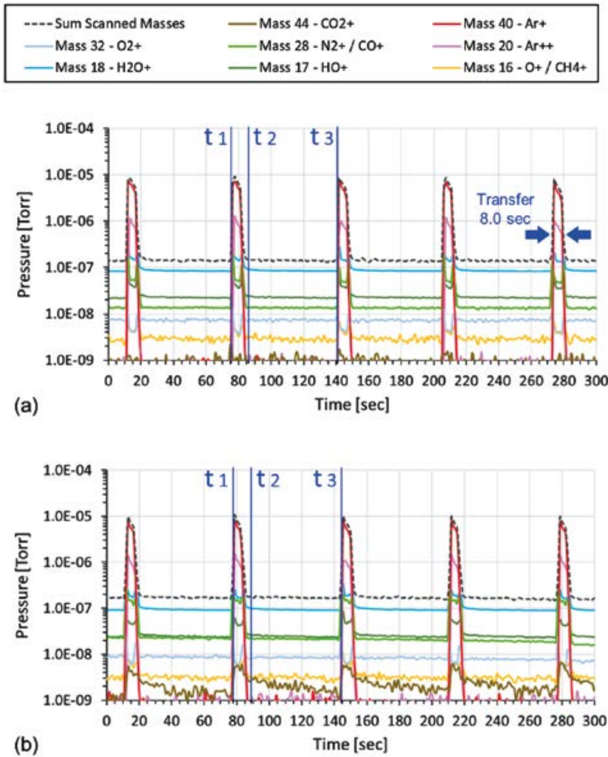


Figure 6: Selected masses measured in the VTM of the HEXAGON system, comparison of SiO_2 wafers (a) vs. PBO wafers (b).

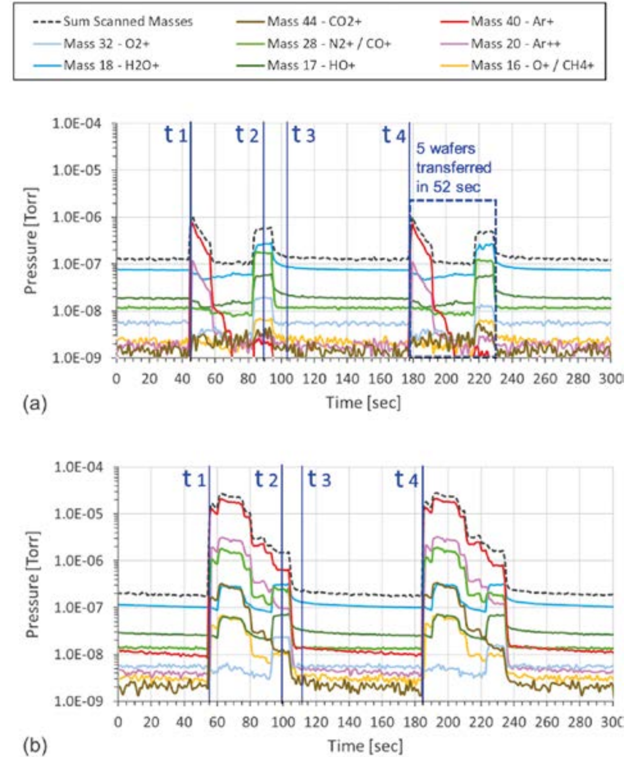


Figure 7: Selected masses measured in the CLUSTERLINE® VTM, comparison of SiO_2 wafers (a) vs. PBO wafers (b).

Time flag	Wafer type	Selected masses and partial pressures [Torr]			
		Mass 18	Mass 28	Mass 32	Mass 44
t_1	SiO_2	1.71E-7	5.76E-8	4.49E-9	9.56E-10
	PBO	2.5E-7	1.61E-7	7.75E-9	4.85E-9
t_2	SiO_2	9.6E-8	1.43E-8	7.3E-9	1.25E-9
	PBO	1.04E-7	2.24E-8	8.19E-9	2.79E-9

Partial Pressures of Contaminants (Data of Fig. 6)

Time flag	Wafer type	Selected masses and partial pressures [Torr]			
		Mass 18	Mass 28	Mass 32	Mass 44
t_1	SiO_2	6.64E-8	1.16E-8	2.6E-9	2.2E-9
	PBO	9.93E-8	1.07E-6	4.66E-9	1.64E-7
t_2	SiO_2	2.71E-7	1.74E-7	1.95E-8	4.22E-9
	PBO	3.12E-7	2.48E-7	2.28E-8	1.27E-8
t_3	SiO_2	9.2E-8	1.18E-8	5.04E-9	1.56E-9
	PBO	1.34E-7	1.39E-8	5.81E-9	2.38E-9

Partial Pressures of Contaminants (Data of Fig. 7)

increase observed at t1, corresponds to the opening of the slit valve of the ICP etch chamber to allow wafer picking. The residual outgassing load impacts the VTM pressure even after the etched wafer is placed to the next process chamber. Initially, in the case of SiO_2 wafers (Figure 7a) only masses 40 and 20 impact the VTM pressure. In contrast, on PBO wafers (Figure 7b) the total pressure is more than one order of magnitude higher and the contribution, beside Ar, comes from all other species, except of mass 32. At the instant t2, a wafer previously degassed in the ABD is picked from the airlock and enters the VTM. This action is accompanied by an increase of the partial pressures of mass 17 and 18, which is likely due to the outgassing of the hot wafer. Similarly, masses 28 and 32 also increase and this can be explained by the residual atmosphere of the airlock. The VTM pressure is again stable at the instant t3; however, there is a much more significant contribution of masses 40 and 20, and in a lesser extent of mass 44, in the case of PBO wafers. This phenomenon was not observed on the HEXAGON (Figure 7b). During steady-state operation, between t3 and t4, one wafer remains idle on the robot arm waiting to be placed in the ICP etch chamber. Since the temperature of this wafer is still around 100°C it continues to outgas and to contaminate the VTM environment. The periodic time interval between t1 and t4 can be used to calculate the steady-state throughput with (1). Thus, a cycle time of 128.7 sec corresponds to a throughput of 28.0 wafers/hour. The throughput limitation comes from the ICP etch sequence bottleneck summed to the overhead due to the chamber-to-chamber transfer.

HEXAGON - PVD-Ti chamber RGA: SiO_2 vs. PBO Wafers

Figure 8a and 8b compare the behavior of the PVD-Ti chamber of the HEXAGON during the residence of SiO_2 and PBO wafers previously processed with ABD, cooling step and split ICP etch. The instant t1, corresponds to the start of the down movement of the pedestal. This is accompanied by a sharp pressure increase caused by the volatile species coming from the other process chambers and by the residual atmosphere of the airlock. After the transfer, in the case of SiO_2 wafers, the total chamber pressure rapidly drops to the level indicated at t2 and remains stable until the next indexing event takes place at t4. Similarly, the contaminant species present remain constant during the timeframe t2-t4. On the other hand, one can notice a slow and steady decay of mass 40 in the same time interval.

In the case of PBO wafers, when the chamber is isolated from the VTM, such as at t2 and t3, the signal of mass 28 and 44 is almost one decade higher compared to SiO_2 (see Table V). Moreover, contrary to SiO_2, mass 40 remains the main contributor to the total pressure. The decay of mass 40 between t2 and t3, is somewhat slower compared to SiO_2. This may indicate that the film material itself and/or the surface roughness plays a role on the incorporation of Ar [15]. It is noteworthy to mention that mass 40 signal would completely disappear at t2 if no ICP etch process would have been performed, but instead only Ar gas would have been flown in the ICP etch chamber (data not shown here). This observation strongly supports the fact that Ar gets trapped in the film during the ICP etch process and is then gradually released over time.

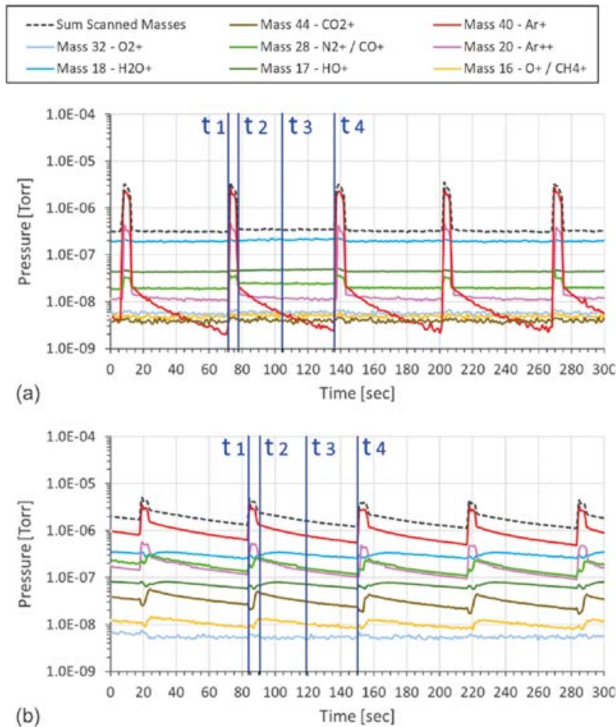


Figure 8: Selected masses measured in the PVD-Ti chamber of the HEXAGON, comparison of SiO_2 wafers (a) vs. PBO wafers (b).

Time flag	Wafer type	Selected masses and partial pressures [Torr]			
		Mass 18	Mass 28	Mass 32	Mass 44
t_1	SiO_2	2.11E-7	3.51E-8	6.66E-9	4.52E-9
	PBO	3.03E-7	1.86E-7	6.12E-9	2.12E-8
t_2	SiO_2	1.94E-7	2.59E-8	5.85E-9	4.45E-9
	PBO	2.96E-7	2.5E-7	5.9E-9	5.01E-8
t_3	SiO_2	2.12E-7	2.43E-8	5.71E-9	3.75E-9
	PBO	3.08E-7	1.55E-7	4.94E-9	2.99E-8

Partial Pressures of Contaminants (Data of Fig. 8)

CLUSTERLINE® – PVD-Ti chamber RGA: SiO_2 vs. PBO Wafers

Figure 9 (a) and (b) compare the RGA spectra measured in the PVD-Ti chamber of the CLUSTERLINE® during the residence of SiO_2 and PBO wafers. The typical base pressure level reached in PVD-Ti chamber reaches values in the low E-8 Torr. Due to the negligible outgassing of the SiO_2 material, when the chamber is isolated from the VTM, (i.e., starting at t1 until t < t4), the base pressure is barely affected by the wafer presence and remains below 5.0E-8 Torr (Figure 9a). The localized pressure instability observed between t1 and t2 is due to the movement of the pedestal from the hand-off position to the process position, which brings the wafer further away from the RGA device. Between t2 and t3, mass 40 exhibits a decay in a similar fashion as described earlier in Figure 8a. During the programmed 50.0 sec of waiting, the pedestal is in the upper position and wafer rests on the chuck top surface. In this so called "process position", the shields assembly restricts the pumping gap. As soon as the sequence time is elapsed, the pedestal moves to the hand-off position, where the pumping path opens and brings the wafer closer to the RGA. This explains the slight pressure increase starting at t3.

The residual outgassing measured on PBO coated wafers is obviously more pronounced compared to SiO_2 (Figure 9b). The total pressure remains to values above 3.0E-6 Torr during the entire residence time until t < t4. The dominating signals are masses 40 and 20, originated from Argon. These are followed, in descending

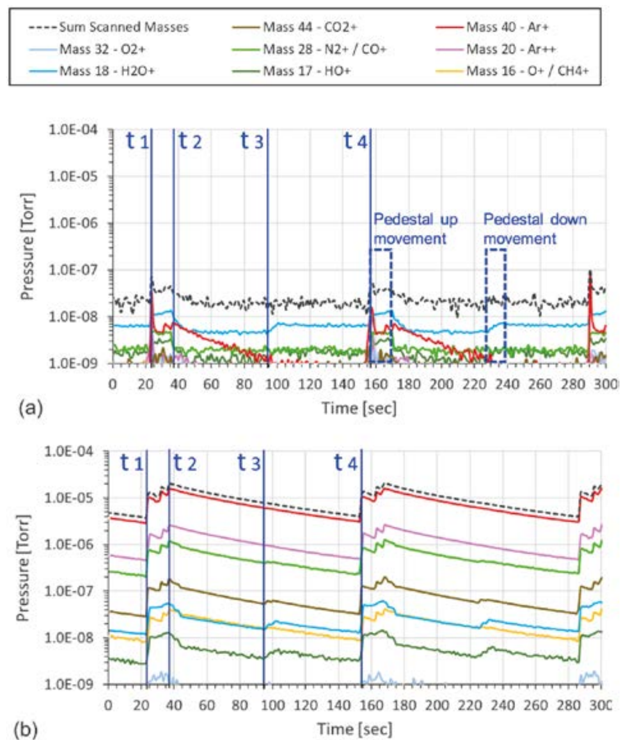


Figure 9: Selected masses measured in the CLUSTERLINE® PVD-Ti chamber, comparison of SiO_2 wafers (a) vs. PBO wafers (b).

Time flag	Wafer type	Selected masses and partial pressures [Torr]			
		Mass 18	Mass 28	Mass 32	Mass 44
t_1	SiO_2	1.23E-8	4.24E-9	1.16E-9	6.69E-10
	PBO	4.4E-8	7.64E-7	1.18E-9	1.17E-7
t_2	SiO_2	1.13E-8	2.37E-9	4.04E-10	8.46E-10
	PBO	5.25E-8	1.17E-6	1.1E-9	1.84E-7
t_3	SiO_2	5.71E-9	1.54E-9	2.38E-10	3.68E-10
	PBO	1.54E-8	3.98E-7	1.4E-10	5.48E-8

Partial Pressures of Contaminants (Data of Fig. 9)

order of partial pressures, by masses 28, 44, 18 and 17 (see Table VI). Similarly, to what observed on the HEXAGON, the rate of decay of masses 20 and 40 is somewhat slower on PBO than on SiO_2.

Summary

During steady-state operation, the VTM pressure of the CLUSTERLINE® is more severely impacted by the outgassing load propagating from the ICP etch chamber and from the etched wafer. This is particularly evident in the case of PBO, where the level of contaminants, especially masses 28 (CO+) and 44 (CO2+), is almost two orders of magnitude larger compared to the HEXAGON tool. Because of the longer chamber-to-chamber transfer interval on the CLUSTERLINE®, the etched wafer may incur in a higher risk of re-contamination from its own residual outgassing. In contrast, the faster and simultaneous wafer transfer in the HEXAGON allows the VTM pressure to recover almost immediately. In this platform, the wafer type plays a less prominent role as indicated by the minor difference in the level of contaminants measured on SiO_2 and PBO.

RGA data from the PVD-Ti chambers of both platforms have shown a very different behavior on SiO_2 and PBO. In general, the contamination caused by SiO_2 wafers is almost entirely due to masses 40 (Ar+) and 20 (Ar++). In the case of PBO wafers, the overwhelming contribution to the total pressure is as well due to masses 40 and 20, but the other contaminants are also present in a significant extent. One interesting difference is that the partial pressure of mass 40 in the CLUSTERLINE® is of order 1.0E-5 Torr, whereas in the HEXAGON it is one decade lower. Some other differences in the magnitude of the volatile contaminants can be distinguished, such as the 50% higher partial pressure of mass 28 (CO+) and mass 44 (CO+) in the CLUSTERLINE® chamber. A possible explanation is the higher wafer temperature reached during the single-step etching process performed on the ICP etch chamber of the CLUSTERLINE®, that in turn causes stronger outgassing in the PVD-Ti chamber. On the other hand, mass 18 (H2O+) exhibits one decade lower partial pressure in the chamber of the CLUSTERLINE®. This significant difference may be explained by the increased efficiency in the pumping of water molecules with the cryo pump, instead of the turbomolecular pump installed on the process chambers of the HEXAGON. The partial pressure of mass 32 (O2+), is situated at approximately 1.0E-8 Torr in the HEXAGON and is not affected by the presence of the wafer in the chamber. Mass 32 is one decade lower in the CLUSTERLINE® chamber. This is in line with the better base pressure conditions.

Conclusion

A quantitative RGA benchmark between the HEXAGON and the CLUSTERLINE® would not be fair due to important HW differences, such as chamber volume, pumping efficiency (cryo vs. turbo in the PVD chambers) and the physical distance between the wafer path and the RGA device. Nevertheless, RGA measured in the vacuum transport module and the PVD-Ti chamber have provided a good picture of the cross-contamination dynamics established during steady-state operation. Experimental data has clearly shown that the main source of contamination in both systems is the residual outgassing load of the etched PBO wafer, that migrates from the etching chamber to the VTM and then accompanies the wafer to the PVD-Ti chamber. Such argument is supported by the very different behavior observed on SiO_2 and PBO films. The former does not exhibit any residual outgassing due to volatile organic contaminants.

A common phenomenon observed in both platforms is the overwhelming presence of masses 40 and 20 in the cloud of volatiles species. This may indicate that a significant amount of Argon becomes trapped in the films as a side-effect of the ICP sputter etch process. During transfer and residence in the PVD-Ti chambers, Argon is then gradually released at a different rate depending on the film material. Although the scale of the Argon presence is very significant, the investigation of the root-cause of this phenomenon is beyond the scope of this paper.

Acknowledgments

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Productivity Boost and Optimum R_c Control in Wafer-Level Packaging enabled by HEXAGON

The megatrend of more miniaturized electronic devices highlights the importance of low and stable contact resistance (R_c). To classify the capability of HEXAGON as High-Throughput UBM/RDL Technology, we report the details of experimental work on throughput and R_c previously presented and published at ECTC 2023 by Evatec's ***Dr. Carl Drechsel***, ***Dr. Patrick Carazzetti***, ***Carl Wang***, ***Dr. Juergen Weichart*** and ***Ewald Strolz***, as well as ***Kay Viehweger*** from Fraunhofer IZM-ASSID (Moritzburg, Germany)[1].

INTRODUCTION

An impressive attribute of the digital transformation are the continuously growing amounts of data being processed. While the average monthly data volume per stationary broadband connection in Germany was only 47 GB in 2015, it had risen to 142 GB in 2019. In 2023 it was already 287 GB, which is about 10 GB per day. However, this does not include the mobile data volume, which averaged 7.2 GB per month in 2023 [2] and might increase tremendously in near future. Although these values differ considerably from country to country, there is nevertheless a clear global trend, which shows the requirement of data capacities that exceed our current average consumption by far: Operating an autonomous vehicle generates for example a data volume of around 5 GB per minute, which would amount to around 7.2 TB (= 7200 GB) per day. And if you want to estimate the amount of data being processed in a Smart Factory, you need to familiarize yourself with dimensions like Petabyte (1 PB = 10^6 GB) or Exabyte (1 EB = 10^9 GB).

The demand for higher data volumes goes hand in hand with a continuous trend for higher performance devices, increasing power efficiency and miniaturization. Recent progress is here explicitly based on wafer-level packaging (WLP) [3], where typically protective layers, electrical connections as well as the packaging itself are implemented before dicing the wafer into single chips. Hence, resulting packages are in similar dimension as the die itself, which is understood as wafer level chip-scale packaging (WLCSP). In advanced packaging this requires multi-layer and fine pitch packaging designs that push the dimensions of vertical interconnects and redistribution layer (RDL) technologies below 5 µm. But since smaller interconnects critically complicate the electrical performance requirements, the control of a low contact resistance (R_c) is becoming more and more important. Additionally, smaller scaling is in state-of-the-art packaging platforms coupled with higher organic loads that needs to be avoided, such as organic or oxide contamination of the metal interfaces.

Here we review hardware improvements that facilitate low R_c results (< 2.0 mOhm) on HEXAGON used in WLP for the creation of under bump metallization (UBM) and RDL. Keeping a low R_c, it is possible to reach a throughput of 80 wafers/hour (WPH). Key drivers for this optimization are an improved airlock design that effectively shrinks pumping and venting times, resulting in a cycle time of approx. 34 seconds per wafer. This allows other processes to be trimmed. Additionally, a new indexer rotation concept of the HEXAGON shortens the chamber-to-chamber transfer, which reduces the risk to re-contaminate the contact pads at the end of the ICP sputter etch step. The electrical performance relevant for R_c calculation is measured on single-contact Kelvin resistors with via diameters from 25 down to 10 micrometers. Experimental data show for all via diameters stable R_c results within a lot of 25 wafers at a high-throughput run of 80 WPH.

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process systems
SEQ 300

I. EXPERIMENTAL METHODS

A. Overview on HEXAGON

To process the wafers, on which later the R_c is evaluated, a high-volume manufacturing HEXAGON platform, especially optimized for boosting the wafer handling speed, has been used. Figure 1 shows the configuration of the HEXAGON system.

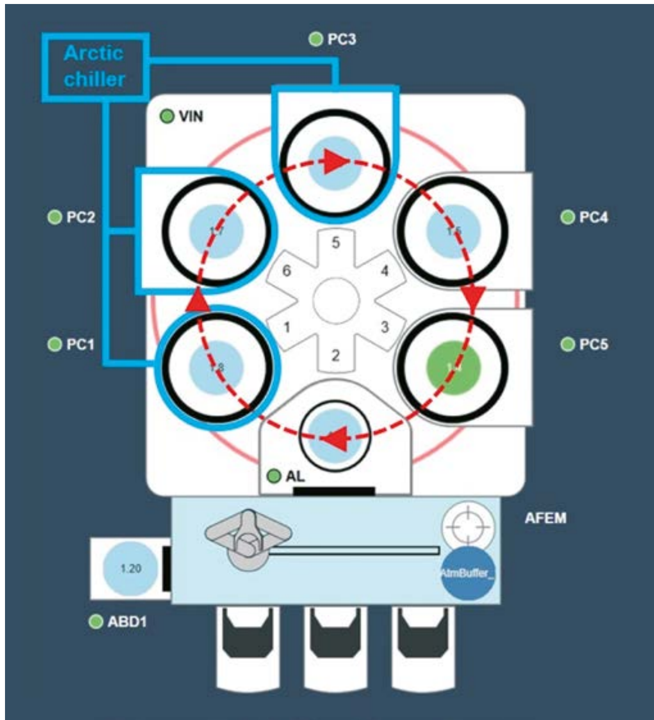

Figure 1: Configuration of HEXAGON platform, indicating pre-treatment (ABD, PC1, PC2, PC3) and PVD (PC4, PC5) modules.

The HEXAGON platform consists of two major components: An atmospheric front-end module (AFEM) and a vacuum indexer module (VIN). The AFEM is equipped with three loadport modules (LPMs) to introduce front opening unified pods (FOUPs) to the system, an aligner to correct eccentricity for every incoming wafer, a buffer as deposit place for pasting wafers and an atmospheric batch degasser (ABD). The VIN is equipped with an airlock (AL) to introduce wafers from AFEM and five process chambers (PCs). PC1 is an arctic cooling station to reduce the wafer temperature between ABD and the two inductively coupled plasma (ICP) sputter etch modules in PC2 and PC3. The ICP sputter etch procedure relies on physical bombardment with Ar+ ions in an ignited Ar plasma. Since ICP sputter etch processes are very critical to the thermal budget, the pedestal and the chamber shields are actively cooled to -30 °C by an external chiller unit. In PC4 and PC5 the PVD process of Ti as adhesion and Cu as seed layer for a final downstream process is performed.

B. Process Description

The procedure of the entire process, performed as BKM on single wafers, is described in Table I. Following the BKM, every wafer is first aligned and next transferred into the ABD, where a degassing phase takes place to avoid adsorbed water molecules on the wafer. There, a batch of 28 wafers can be processed simultaneously while a laminar N2 flow guarantees constant peak temperatures on the wafers, independently of the position and the total number of wafers loaded. The total degassing time and temperature is product specific and typically ranges 20-30 minutes and 120-130 °C. After degassing, wafers are transferred to the AL and thus get into the VIN. Next, they enter the first process chamber (PC1) and cool down to roughly half of the ABD peak temperature. This is important to ensure that the thermal budget of the ICP sputter etch process in PC2 and PC3 starts from a preferably low point. Since etching gives the highest amount to the thermal heat on the substrate, the total etch amount required is equally distributed to PC2 and PC3. In addition to pure Ar+ ion bombardment, the entire etching process also includes in-situ cooling and purging steps to reduce the peak temperature. After finishing the etching and the Ti/Cu PVD in PC4 and PC5, the wafers get back to AL and are therefrom re-transferred to the FOUP.

Module	Physical process
LPM	FOUP is loaded to the AFEM & Wafer is taken
Aligner	Eccentricity check & notch alignment
ABD	20-30 min degassing at 120-130 °C
AL	Wafer is transferred from AFEM to VIN
PC1	Cooling to ≈ 50 % of ABD temperature
PC2	15 nm removal by ICP sputter etch
PC3	15 nm removal by ICP sputter etch
PC4	100 nm Ti PVD
PC5	300 nm Cu PVD
AL	Wafer is transferred from VIN to AFEM
LPM	Wafer is put back & FOUP is unloaded from AFEM

Table 1: Overview of BKM process flow

C. R_c Measurement

The R_c measurements are performed on four-terminal Kelvin resistors, built on 300 mm Si wafers. An overview of all steps necessary for the completion of a full R_c test vehicle is illustrated in Figure 2.

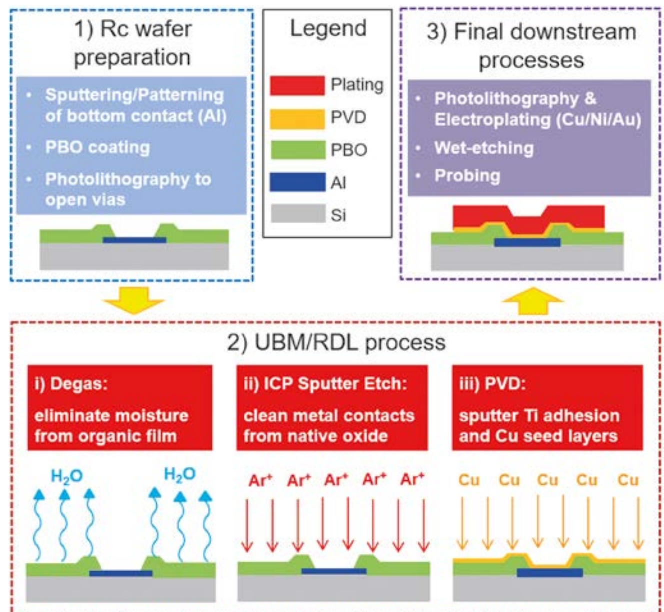

Figure 2: Fabrication flow indicating process steps of Rc test vehicles on 300 nm Si wafers.

Each R_c test vehicle consists of a patterned metallization layer (1 µm sputter-deposited Al) on a Si substrate, which acts as basic redistribution line (RDL0). On top of that a 9 µm thick passivation film of PBO is deposited. By means of photolithography, a contact opening via is created on top of the RDL0 (see Figure 2, step 1). The smaller the diameter of the opening pad d0, the more sensitive to the R_c is the Kelvin resistor. This is followed by the BKM flow (see Figure 2, step 2). Cleaning the pads and depositing Cu as RDL1 without oxidation is essential for an optimum operation of the device and is revealed by a low Rc. Next the final downstream process follows, which includes a thickening of RDL1 by 3 µm Cu electroplating and an addition of 2 µm Ni and 0.5 µm Au by selective plating of the probing pads to improve the reliability of the latter R_c measurement (see Figure 2, step 3).

An enlargement of a test vehicle used for this study and a sketched cross section of an opening via is shown in Figure 3. Each test vehicle has a total number of 121 cells, containing series of Kelvin structures differing in via diameter (d0), overlap size between RDL0 and RDL1 that is equal to 0.5(d1 – d0) and connector width c. The R_c measurement is performed at a voltage in the order of 1 mV with a vertical probe card. It is leveled by a fully automatic probe station (TEL Precio) and the high-precision measurement is conducted by an Advantest V93k test head with analog VI cards. A detailed description of the measurement procedure and calculation of the R_c can be found in [4].

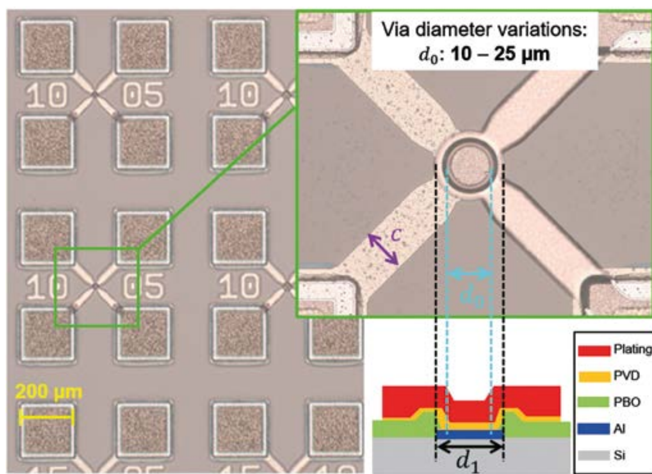

Figure 3. Enlargement of Rc test vehicle with four-terminal Kelvin resistors

As standard qualification procedure, for each experiment condition, a lot of 25 wafers is processed with the described BKM. Before the lot is started, a single Al pasting wafer is etched for 90 s to ensure similar conditions in PC2 and PC3. PC4 and PC5 are warmed up with PVD processes on 4 dummy wafers. In the lot, the R_c test vehicles are located in slots 1, 13 and 25, while all other slots are filled with PBO dummy wafers.

II. HARDWARE FEATURES OF HEXAGON

The optimized, high throughput of HEXAGON is the consequence of a very short cycle times. The cycle time itself can be divided into handling time and process time.

The handling time denotes the duration a PVD system needs to transfer all wafers to the next process chamber between completion of the last process and start of the next process. In an indexer system, it consists of a synchronized downward pedestal movement, a 60° clockwise rotation of the indexer carousel and an upward pedestal movement.

The process time is product specific and depends mostly on the required etch amount and PVD thicknesses. However, in standard applications of UBM/RDL deposition, the etching sequence is usually the process time bottleneck. Within the ICP sputter etch sequence, there is also time for pumping and purging before and after pure etching in order to prevent contamination of the etched pads and to keep the thermal excursion as low as possible.

A. Optimized Indexer Unit

The reduced handling time of HEXAGON has its origin in the design of the central rotating device. While in previous indexer systems the support paddles on the indexer carousel were connected to a motor by gears (see Figure 4a), the new design places the paddles directly on the rotary table driven by a central servo motor (see Figure 4b). Only this causes a time gain of approx. 2 s. Additionally, the potentially higher attrition of the gear wheel components is counteracted. The total handling time was shortened to approx. 9 s.

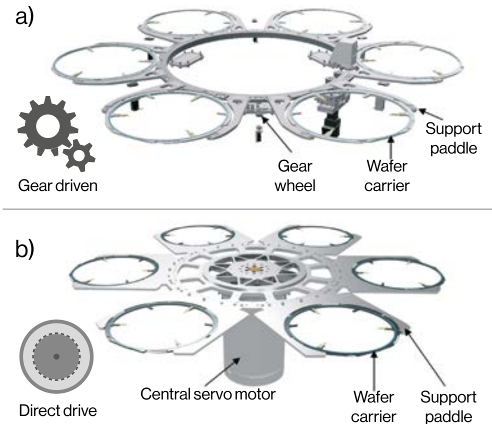

Figure 4. Comparison between previous and new design of central rotating device; a) previous gear driven indexer unit; b) new direct drive approach.

B. Optimized Airlock Cycle

HEXAGON also uses an optimized AL design. Compared to an earlier indexer tool design, the AL volume V0 has been reduced to 25%. Instead of one large turbo pump, two smaller ones, each with its own pump valve, are installed (see Figure 5).

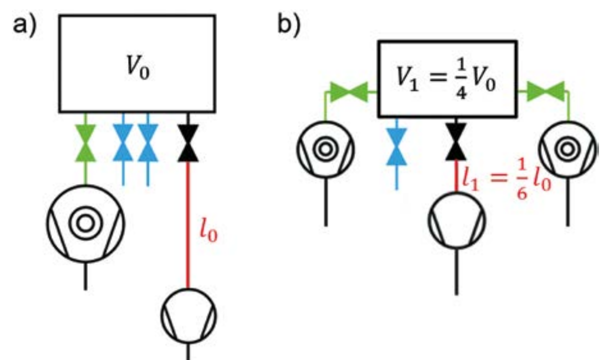

Figure 5. Scheme of AL in a) previous design and b) new design. Different colors indicate pumping valves (green), venting valves (blue) and fore-vacuum valves (black). The pumping line to fore-vacuum pump is marked in red.

Furthermore, the pump line l0 between the fore-vacuum valve and the roughing pump was shortened by mounting the roughing pumps directly on the main frame of the tool. All in all, this enabled the pumping time to be roughly halved. The number of venting valves at the AL has been reduced from 2 to 1, since the reduction of the AL volume does not require more venting capacity. Even so, the venting time at AL is also reduced by about half.

By the optimization of AL, a cycle time of approx. 34 s can be reached, which corresponds to a peak throughput of approx. 105 WPH when the system runs in dry-cycle mode. A pressure-time analysis of the AL, including pumping, handling time, venting and wafer exchange is illustrated in Figure 6.

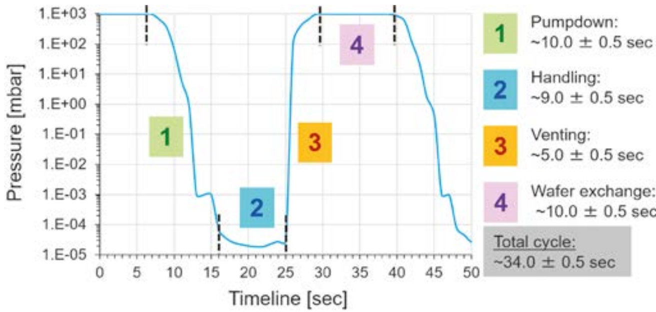

Figure 6. Pressure vs. time analysis of a single AL cycle time.

III. THERMAL MODEL AND R_c ANALYSIS

A. Thermal Model

The temperature flow over the whole BKM stack can be simulated with a thermal model [5]. Applying it to throughputs of 44.2, 54.5, 69.2 and 80.3 WPH (see Figure 7), allows to determine the peak temperature after ICP sputter etch process and over the full stack process. From this, a correlation between peak temperatures and the respective throughput can be determined (see Figure 8).

B. R_c Analysis

For all throughputs, on which the thermal model is applied, the R_c is measured on a lot of 25 wafers. It indicates on which values and how constant the R_c remains in the face of higher chamber temperatures during continuous operation. Figure 9 shows for different throughputs the averaged result for via diameters of 10, 15, 20 and 25 µm on wafers in slots W#1, W#13 and W#25.

All R_c results for investigated throughputs are in the order of 1-2 mΩ. Only the run at 44.2 WPH shows higher values at a via diameter of 10 µm for wafers #13 and #25. Regarding to the examined via diameters, a larger diameter generally leads to lower R_c values. Within a FOUP, the R_c values remain extremely stable at 80.3 WPH, while a slight increase can be observed at 69.2 WPH and a significant increase at 44.2 WPH. For 54.5 WPH the R_c values even decrease very slightly. The statistical error ranges are very small for the measurements with via diameters of 20 and 25 µm, for 15 µm they are a bit larger. For 10 µm, on the other hand, the error ranges are more than twice as large. This arises from the systematically more inaccurate measurement conditions for smaller via diameters.

Overall, the R_c results for high-throughput runs on HEXAGON reach a very low level (< 2 mΩ). Although the peak temperature is highest at 80.3 WPH (see Figure 9), no negative impact on the R_c behavior can be detected, which is attributed to faster process and handling times, reducing the potential time for a recontamination of the etched pads.

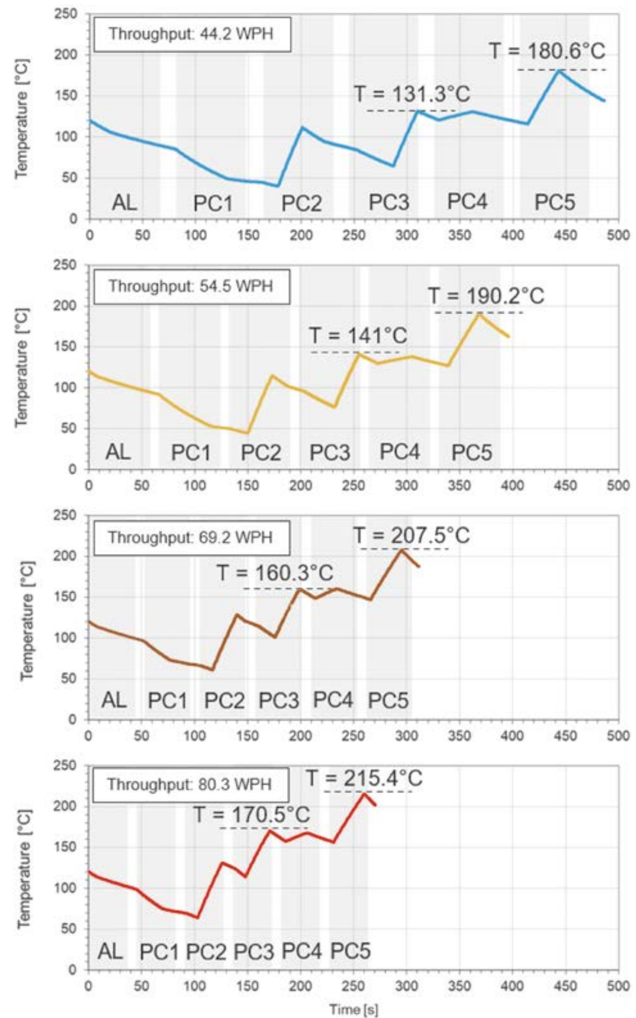

Figure 7. Thermal model for different throughputs, indicating the maximum temperature after ICP sputter etch and for the entire process.

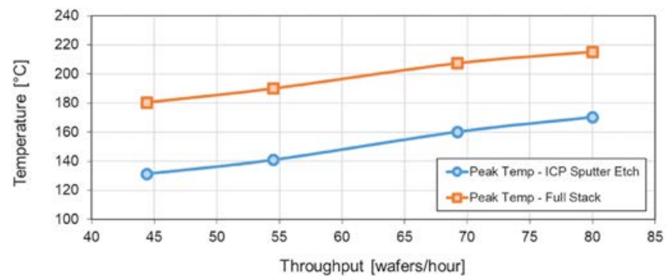

Figure 8. Peak temperatures after ICP sputter etch process and within total stack for different throughputs.

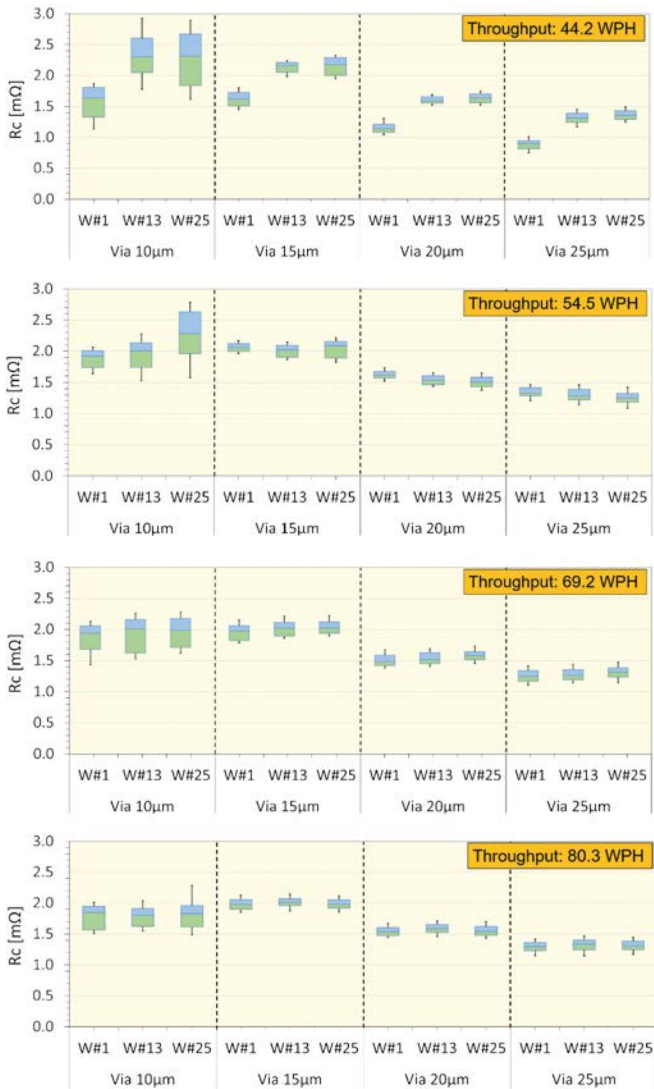

Figure 9. Rc results for different throughputs and via diameters. W#1, W#13 & W#25 indicating the slot position of the test wafer within a FOUP.

CONCLUSION

Due to continuous miniaturization in high-end and advanced packaging, the control of R_c has uttermost importance. In this work we discussed the achievement of low R_c results on a HEXAGON system used for UBM/RDL in WLP. At the same time, the throughput is increased to 80 WPH based on hardware improvements.

The hardware optimization can be divided into a new design of the central rotating device and the AL. The first leads to a reduction of the handling time, the second leads to a reduction of the AL cycle time, i.e. the duration the AL needs to pump down, handle, vent and exchange a wafer. Based on experimental data, the R_c was measured for throughputs between 44.2 and 80.3 WPH on single-contact Kelvin resistors with via diameters of 25 down to 10 µm, located in the 1st, 13th and 25th slot of a FOUP. Furthermore, the temperature profile of a test wafer was simulated for all throughputs, from which the peak temperature after etching process and for the full stack process is determined.

It could be proven that an increase in throughput is associated with an increase of the peak temperatures, but at the same time no increase in R_c is observable. In particular, the via diameters of 10 and 15 µm show a lower R_c at high throughput. The comparison of the R_c results for the 1st, 13th and 25th wafer exhibits no increase for wafers within one full lot. In summary, we provide evidence that an increase in throughput on a HEXAGON platform goes hand in hand with an optimum R_c control. This performance is achieved even though the full stack peak temperature exceeds 215 °C.

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Advances in Frontside Process Technology: Trench/Via Filling & Planarization

Trends in frontside contact formation in new power device technologies on Si or SiC are calling for ever more demanding thin film processes – trenches get deeper, aspect ratios get higher and expectations for the quality of the final planarized surface grow. Evatec's Product Marketing Manager ***Fabian Kramer*** and Manager of Technology Development ***Mohamed Elghazzali*** give us a taste of the Evatec solutions supporting customers in 2025 and beyond.

The process requirements are clear

Trench/Via filling and planarization processes call for deposition of two layers.

1. A "seed" layer with good step coverage – typically comprising a thin titanium layer in the range 20-50 nm followed by a TiN layer in the range 150-250nm. The Ti layer acts as adhesion layer and TiN as barrier layer.
2. A thick metal contact layer, typically Al , AlCu or AlSiCu according to the device design in the thickness range between 3000-5000nm. The process conditions need to ensure good flow of the material within the trench without voids and provide good final planarization.

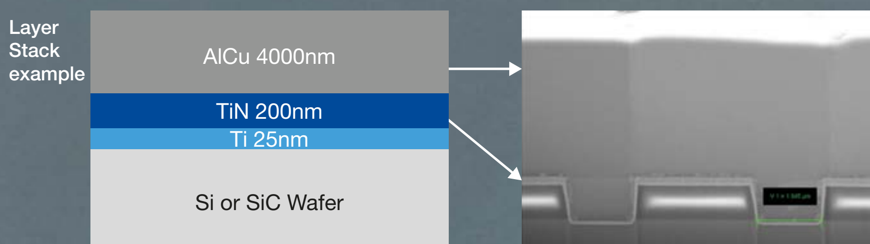
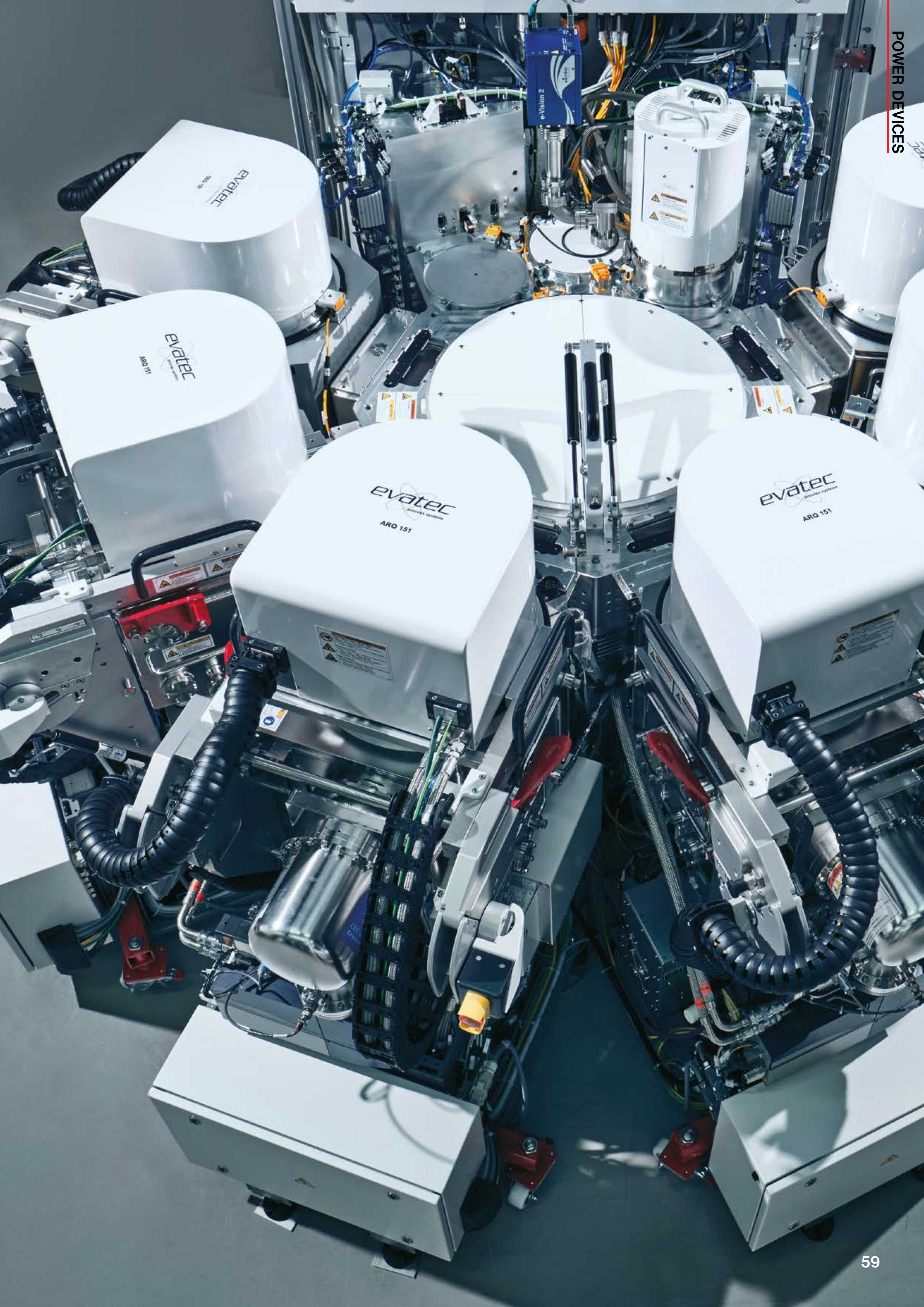


Figure 1: CLUSTERLINE® 200 results for trench filling and planarization

> *"Supporting Perfect Al Flow in higher aspect ratio trenches"*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CLUSTERLINE® solutions are already well established

Evatec's CLUSTERLINE® 200 and 300 platforms are already well established in power device applications.

Figure 1 illustrates a micrograph of typical results achieved on CLUSTERLINE® 200 for frontside contact formation with trenches of aspect ratio approximately 1:1. Seed layers provide the step coverage required for good aluminium adhesion, while good material flow at process temperatures around 400ºC provides the required void-free films with smooth surfaces. Details of a typical single process module are shown in Figure 2.

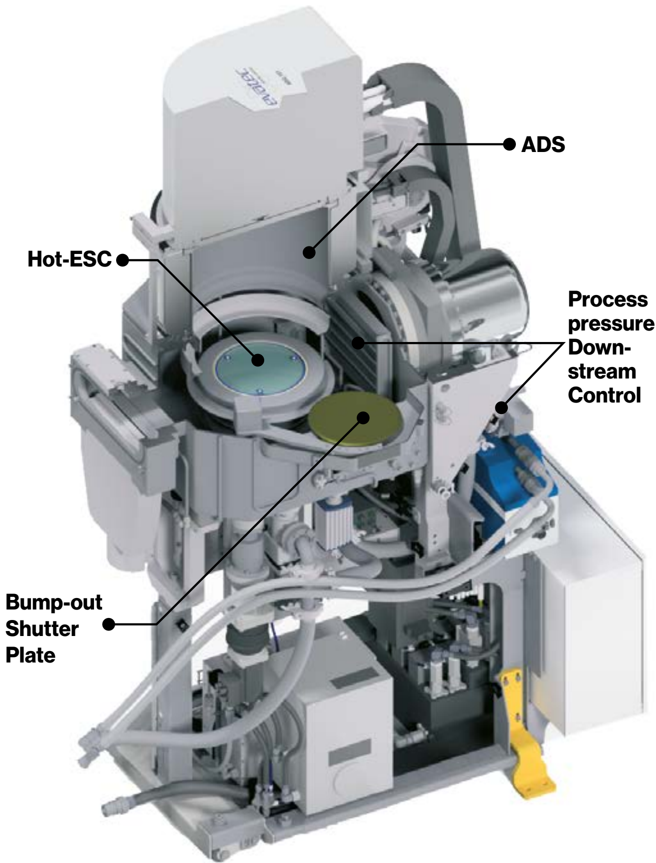

Figure 2: Single process module

More challenging process demands are coming in 2025

Emerging trends in device architecture calling for higher aspect ratios are setting more demanding challenges for substrate handling and thin film processes.

Seed layer deposition needs to achieve sufficient side wall and bottom coverage without significant increase in overall film thickness. For the thick metal layer deposition, substrate handling within the process chamber needs to avoid "sticking" and the risks of subsequent damage or particle generation, while Al Flow still needs to ensure void free films for the more demanding device architectures.

New solution to achieve a higher aspect ration of 3:1

New dedicated hardware and process control features being introduced to the market at the end of 2024 for CLUSTERLINE® 200 will enable our customer to achieve the new levels of process performance for high aspect ratio features.

- Enhanced new module design for Advanced Directional Sputtering (ADS) will deliver the improved step coverage essential for higher aspect ratio trenches without increasing required TiN film thickness and deposition times.
- Process module control technology leveraging downstream pressure control will deliver enhanced process control and process repeatability for the reactive processes required in TiN deposition for the most consistent seed layer deposition in higher aspect ratio applications
- New process kits including integrated substrate shutters and modified shielding will bring further benefits:
  - Elimination of any wafer pasting steps required simplifying processes and increasing wafer throughput
  - Improved particle management
- New full face Electrostatic Chuck (ESC) for efficient thermal coupling will enable process temperatures up to 500ºC, which will offer customers wider process windows for any new processes and reduce risk of wafer sticking and edge damage.

CLUSTERLINE® 200 is the solution

CLUSTERLINE® 200 enables integration of up to 6 process modules. A possible system layout for front side contact metallization integrating these new capabilities is shown in Figure 3.

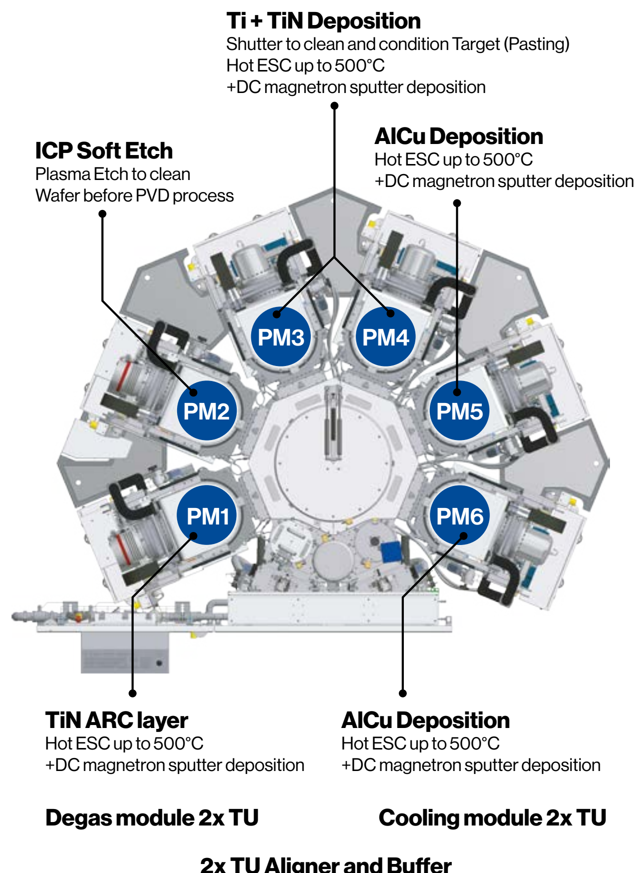

Figure 3: Typical CLUSTERLINE® 200 configuartion for gap filling and planarization

SPOTLIGHT ...CLUSTERLINE® 200

A choice of architectures

The CLUSTERLINE® 200 can be configured as a tool for single substrate or batch processing using Single Process Modules (SPM) or a Batch Process Module (BPM) respectively. However, when you configure the tool, you can rely on fully automated cassette-to-cassette processing using Evatec's proven safe handling. For custom applications please also enquire about configurations combining both single and batch process modules.

SPM configuration highlights

Platform variant with strong pedigree in Power Devices, Advanced Packaging, MEMS and Wireless markets allowing easy tool configuration and future expansion for PVD, highly ionized PVD, Soft Etch, PECVD and PEALD for wafer sizes up to 200mm.

- Modular chuck design for rapid exchange between 100, 150 or 200mm formats for production flexibility and maximum tool utilization
- Up to 6 single process modules and up to 6 auxiliary modules for pre- and post treatment steps
- Auxiliary module functions including wafer alignment, buffer, degas, cooling, and ID reader
- Direct thin wafer handling and processing capability for substrate thicknesses down to 70 microns

BPM configuration highlights

Platform variant combining the benefits of sputter batch processing with completely automated handling for selected applications in MEMS and Wireless. A true work horse in the LED / Micro Display and Photonics industries. Integration of additional plasma sources opens up process possibilities for enhanced deposition processes e.g. coating modification including gap filling and planarization.

- Batch processing of up to 20+1 six inch substrates simultaneously
- Batch processing of up to 15+1 eight inch substrates simultaneously
- Rotating substrate table with option for individual rotating substrate chucks
- Integration of up to 4 PVD sputter sources plus 1 plasma source

Want to know more?

To learn more about upcoming solutions on CLUSTERLINE® 200 for power, front or backside applications contact your local Evatec office.
https://evatecnet.com/about-us/contact-us/

Not familiar with the CLUSTERLINE® platform? Then why not watch the short CLUSTERLINE® family video to learn about Evatec's range of solutions for 200, 300 and 600mm.

Power ICs: New Cu Frontside processes on 300mm

PVD Manager Technology Development ***Mohamed Elghazzali*** tells us why Evatec's CLUSTERLINE® 300 is the ideal platform to satisfy the growing demand for 300mm processing and how Evatec process know-how is delivering high performance thick copper layers.

Why copper technology

Silicon-based devices need to improve to stay competitive from a cost and performance perspective. To achieve this, silicon power device production is moving from 200mm to 300mm wafer size and aluminum contact technology is being substituted by copper. In comparison to aluminum, copper provides higher electrical conductivity which results in lower losses and a lower Rds-on (Drain – source on-resistance). Most importantly copper is the technology of choice for Si CMOS today: A power device in copper is compatible with the front end of line processes, enabling direct integration in complex IC packages, e.g. BCD, Power IC.

Aluminum based devices are assembled by solder contact, limiting the flexibility for integration. Complex devices with higher integration require advanced packaging solutions, e.g. flip chip bumping. Advanced packaging solutions based on copper technology are the enabling solution for higher integration density (system in package, embedded dies etc.) and increased energy efficiency.

CLUSTERLINE® 300 – A platform built for front side processes

CLUSTERLINE® 300 is designed for the contamination-free processes and the low particle levels required for front side processes on 300mm. For typical Tungsten-Titanium-Alloy and thick copper single layer processes customers can expect WiW thickness / resistivity uniformities (max,min) <5% (1 Sigma <2.5%) across a 300mm wafer with edge exclusion of 3mm.

CLUSTERLINE® 300 can be configured with up to 6 process modules for degas, deposition or etch. Up to 3 load ports / FOUPS deliver wafers to the Atmospheric Frontend Module (AFEM) equipped with robot and aligner with additional options for integration of wafer buffer stations and additional Interface modules (e.g. high pressure cool). Evatec's highly efficient atmospheric batch degas (ABD) technology developed for the highest throughput Fanout and WLCSP processes is also just one of the additional capabilities that can be added for custom applications.

PVD Technology for WTi/Ti-Cu Processes

Evatec's proprietary PVD module technology is at the heart of the tool. The module enables flexibility in process geometry with target substrate distances in the range of 50 to 80mm. Hardware features focused on maintaining stable process pressures and uniform gas distribution combined with low arcing deliver the process stability and repeatabilities required for high volume production. The limited thermal budget of the substrates necessitates strict control of temperature throughout the entire 5 to 10 µm film deposition process. The principal characteristics of the recently developed cold ESC system ensure that the temperature of the wafer remains below 150°C. This has the beneficial effect of reducing the wafer bow to below 350 µm at a film stress of approximately 180 MPa. In conjunction with the specially designed cathode, this results in the ability to manage high power processes, enhancing overall productivity and providing a reliable processes with minimal in-film particle performance.

Film parameter	Performance
Thickness	5... 10µm
Deposition rate	>25 nm/s
WiW thickness uniformity	<5% (Max/min)
WiW RS uniformity	<5% (Max/min) (@ 500nm thickness)
WtW thickness uniformity	<2% (Max/min)
WtW RS uniformity	<2% (Max/min) (@ 500nm thickness)
Specific resistivity	2 ±0.3 uOhms*cm
Average film stress	app. 180 MPa
Max. wafer bow @5µm @10µm	app. 280µm app. 560µm
Max. wafer temp @5µm @10µm	<100ºC <130ºC
Mech. particles >0.16µm	< 10 adders
In-film particles >0.20µm	< 30 adders

Figure 1: Typical WTi process performance data

> *"Enjoy lower losses and drain source resistance with copper technology"*

Lets take a look at the results

Evatec process know-how optimizes the overall process. Cathode and new developed Cold ESC chuck technologies are designed to enable maximum deposition rates for the highest throughput whilst still maintaining low substrate temperatures. Deposition conditions for both barrier and copper layers are tailored to manage overall film stack stress.

- **WTi deposition**
  Film performance data of typical WTi films in the range 50 to 200nm deposited using Evatec's PVD cathode technology is shown in Figure 1. Processes can be wide ranged tailored for either compressive or tensile film stress according to customer preference.
- **Thick Copper Layer Deposition**
  Layer performance for copper films typically in the range 5 to 10 microns is illustrated below in Figure 2. Films typically display low levels of tensile stress.

Particles and process repeatability performance

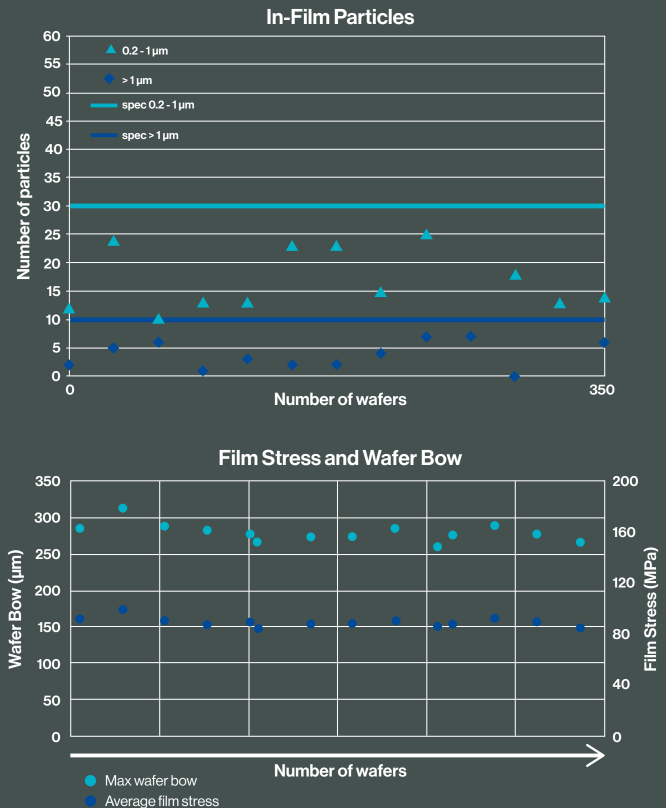

Figure 2: Thick copper deposition process stability

Low-field transport properties and scattering mechanisms of degenerate n-GaN by sputtering from a liquid Ga-target

Dr. Philipp Doering, from Fraunhofer Institute for Applied Solid State Physics (IAF) & *Thomas Tschirky*, Evatec Senior Scientist talk about the work being done on sputtering from a liquid Ga-target.

Abstract

In this work, degenerate n-type GaN thin films prepared by co-sputtering from a liquid Ga-target were demonstrated and their low field scattering mechanisms described. Extremely high donor concentrations above 3×10^{20} cm^{-3} at low process temperatures (< 800 °C) with specific resistivities below 0.5 mΩcm were achieved. The degenerate nature of the sputtered films was verified via temperature-dependent Hall-measurements (300-550 K) revealing negligible change in electron mobility and donor concentration. Scattering at ionized impurities was determined to be the major limiting factor with a minor contribution of polar optical-phonon scattering at high temperatures. Scattering at dislocations or grain boundaries was ruled out to impact the measured mobility. The results demonstrate the huge potential of sputtering as an alternative route for the realization of low-temperature, high throughput and large-scale, regrown n-type GaN.

The use of GaN-based low-noise and high-power amplifiers as well as their advanced hetero-integration into conventional Si-CMOS technology are of major interest for next generation wireless communication systems. To meet the increased data rate requirements, higher frequencies with improved efficiency and bandwidth are targeted. However, further downscaling of the gate-length (L_G) to address higher cutoff frequencies requires significant reduction of parasitic resistances in the devices.

The access resistance of highly-scaled high-electron mobility transistors (HEMTs) or multi-channel devices suffer from the inherent metal-semiconductor barrier for high Al-content barriers. A current transport mechanism completely determined by tunneling is desirable to achieve the lowest possible voltage drop at the metal-semiconductor interface. Removing the AlGaN-barrier and/or rendering the sub-contact area n-type is the only possibility to change the electron transport across the barrier to the 2-dimension

View of the liquid Ga target through the wafer holder in the prototype sputter module

Sample	Substrate	$t_{n\text{-}GaN}$	T_H	GR	rms	FWHM (00.2)
A	GaN/Sapphire	150 nm	700°C	0.9 nm/s	0.58 nm	0.188°
B	GaN/Sapphire	150 nm	590°C	0.9 nm/s	0.38 nm	–
C	GaN/Sapphire	150 nm	800°C	0.9 nm/s	0.91 nm	0.134°
D	Sapphire	1050 nm	800°C	0.6 nm/s	21.6 nm	0.437°

Table 1: Structural properties of co-sputtered n-GaN: $t_{n\text{-}GaN}$ – thickness of Si-doped GaN-layer, T_H – nom. Heater temperature, GR – growth rate, rms – root mean square, FWHM - full-width half maximum of the 00.2.

electron gas (2DEG) from a thermionic to field-emission type at higher Al-contents. However, to achieve the high doping concentrations ($N_D > 1\times10^{20}$ cm^{-3}) for a completely field emission based current transport is difficult due to the decreasing crystal quality. In addition, low temperature processes on a large wafer scale are beneficial to protect the AlGaN/GaN-interface in a HEMT or for a direct III-Nitride hetero-integration of (opto-)electronic devices on a Si-based platform.

In this work, the transport properties of heavily Si-doped GaN thin films deposited by co-sputtering from Si and a liquid Ga-target and on 4-inch sapphire substrates are investigated. Extremely high effective donor concentration ($N_D > 3\times10^{20}$ cm^{-3}) are demonstrated. Specific resistivity below 0.5 and 3.5 mΩcm are achieved at growth temperatures of 800°C and 590°C, respectively. Carrier mobilities were found to be limited by scattering at ionized impurities at the high Si doping levels. Donor-acceptor compensation ratio was found nearly constant below $\Theta \approx 0.2$ even beyond $N_D > 1\times10^{20}$ cm^{-3} different to reported data by metalorganic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE). Temperature-dependent Hall-measurements revealed negligible change in carrier density and mobility with increasing temperature indicating Mott-transition from a semiconducting to a metallic character. Carrier densities and specific resistivity at low growth temperatures (≤ 800 °C) are found well beyond reported data of MOCVD-grown thin films. The results demonstrate the feasibility of sputtered GaN from a liquid Ga-target as alternative process with high carrier density and easy upscaling beyond 4-inch suitable for future process integration into future radio-frequency or optoelectronic (e.g., tunnel junctions) GaN-based devices.

Recent focus on the development of advanced contact processes is generally driven by CMOS-compatible, Au-free and/or low temperature budget ohmic contacts, or n-GaN regrowth for highly-scaled AlGaN or novel Al(Sc)N-based HEMTs with high Al-content. The fabrication of highly n-type doped GaN films was demonstrated via Si-implantation, MBE, MOCVD (Si or Ge), pulsed laser deposition (PLD) and reactive, pulsed sputtering (PVD) from a solid Ga-target (Si, Ge, Sn, O). Si-implantation is used for GaN-devices but faces issues to achieve carrier densities above 1×10^{19} cm^{-3} and requires a high-temperature treatment to recover for the implantation damage. MBE-regrown ohmic contact layers are currently the method of choice due to the low growth temperature but faces issue in terms of upscaling, throughput and homogenitiy. MOCVD regrowth was demonstrated via flow-modulation epitaxy at low growth temperatures with reduced growth rate, but faces limitations in terms of achievable carrier density beyond 5×10^{19} cm^{-2} at 550 °C and does not offer a non-selective growth mode to avoid growth rate inhomogeneities. Typical growth temperatures with high growth rates are conducted at much higher temperatures (> 950 °C). Reactive sputtering was demonstrated with high carrier density and high mobility on 300 – 600 nm thick films. However, the used solid Ga-targets need to be heavily cooled to remain solid during sputtering. In addition, the cooling system gets more complex for larger wafer diameters and impurity concentration in e.g., ceramic Ga is not easy to handle. The use of a liquid Ga-target avoids the need of a complex cooling-system required to keep solid Ga-targets below its melting point. The liquid target can be easily filled up and no sputter craters occur during growth. In addition, the liquid target can be easily upscaled to larger wafer diameters (> 2-inch) as well as lower unintentional/parasitic doping occurs when compared to a ceramic Ga-target.

4-inch sapphire substrates were used for the deposition of the conductive thin films. Three samples (A-C) were initially grown by metal-organic chemical vapor deposition with an Fe-doped buffer to render the GaN-layers semi-insulating topped with a 200 nm unintentionally-doped GaN layer to compensate for Fe-segregation. The sheet resistance of samples A, B and C were measured after MOCVD buffer growth via contactless Eddy-current revealing a $R_S > 100$ kΩ/sq, which is the upper measurement limit of the setup. GaN films were deposited by co-sputtering of a Si-bar and a liquid Ga-target in an Evatec CLUSTERLINE® 200II with a modified process module. 150 nm Si-doped GaN were sputtered on top of the MOCVD-GaN with nominal growth temperature of 590, 700 and 800 °C. Sample D was prepared by directly sputtering GaN:Si on Sapphire. Rocking curves of the 00.2-reflex were carried out by X-ray diffraction to determine the full-width half maxima (FWHM). FWHM were derived from fitting of two pseudo-Voigt functions assuming that the peak with lower intensity is related to the sputtered, Si-doped GaN. The FWHM of the MOCVD-grown buffer was found to be FWHM = 0.064°. Fitting of the sample with lowest growth temperature was not possible due to the low intensity of the second peak. However, it can be concluded that lowering the heater temperature leads to a slight decrease in crystal quality.

Atomic force microscopy (AFM) was used to determine the root mean square (rms) to revealing smoothest surface morphology with lowest growth temperature. A summary of the structural properties is given in Table 1.

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The theoretical metal-semiconductor transport properties (thermionic emission - TE, thermionic field emission - TFE; field emission – FE) are dependent on the characteristic energy E_{00}, which in turn is dependent on the carrier density in the sub-contact area as following:

$$E_{00} = \frac{qh}{4\pi}\sqrt{\frac{N_D}{\varepsilon_r\left(\frac{m_{tun}^{*}}{m}\right)}}$$

With q, h, ε_r (9.5), m_{tun}^* and m ($m_{tun}^*/m = 0.22$) are the elementary charge, Plancks constant, relative dielectric constant, effective tunneling mass, and electron mass, respectively. We use the simple differentiation: FE: $E_{00} \leq 0.5\,kT$; TFE: $0.5\,kT \leq E_{00} \leq 5\,kT$ and $E_{00} \geq 5\,kT$. Thus, to achieve $E_{00} \geq 5\,kT$ a donor concentration of $N_D > 1\times10^{20}\,cm^{-3}$ is required for GaN. Fundamental low-field transport properties are characterized by Hall-measurements at room-temperature (RT). Ti-based ohmic contacts were evaporated via shadow masks and 4-terminal structures mechanically isolated. The use of a co-sputtering of a Si-bar comes along with the possibility to achieve a gradient in Si-concentration over the same wafer depending on the distance of the wafer area to the Si-bar. Thus, several carrier concentrations and corresponding carrier mobilities can be measured on the same wafer. Carrier densities of $N_D = 6.7\times10^{19}$ to $3.7\times10^{20}\,cm^{-3}$ with carrier mobilities of $\mu = 21$ to $42\,cm^2/Vs$ were found over all samples. Improved compensation ratios were found with increasing heater temperature as given in Figure 1. The achieved carrier densities are well beyond the state of the art reported for MOCVD ($N_D < 2.2\times10^{20}\,cm^{-3}$) and MBE ($N_D < 2\times10^{20}\,cm^{-3}$) at generally lower growth temperature (Figure 1c). The achieved carrier densities are exceeding the the $E_{00} \geq 5\,kT = N_D > 1\times10^{20}\,cm^{-3}$ requirement described before. In addition, the extremely high carrier concentrations would be well suited e.g., to address source starvation issues causing linearity distortion in highly scaled GaN-HEMTs.

In general, several scattering mechanisms could be assumed for the co-sputtered GaN:Si even though impurity scattering is most likely dominating at high donor concentrations. Scattering at ionized impurities in dependence of the compensation ratio $\Theta = N_D/N_A$ can be expressed by:

$$\mu_{II} = 3(\varepsilon_0\varepsilon_r)^2\left(\frac{h}{q}\right)^3\left(\frac{n}{N_I}\right)\left(\frac{1}{m^*_F}\right)\left(ln(1+\beta_F{}^2) - \frac{\beta_F{}^2}{1+\beta_F{}^2}\right)^{-1}$$

With:

$$\beta_F{}^2 = \frac{16m^*_e\varepsilon_0\varepsilon_r E^2{}_F}{3q^2h^2n}$$

And N_I and m^*_F are the ionized impurity concentration and effective mass at the Fermi energy, which is given by:

$$m^*_F = m^*_e\left(1 + \frac{6\alpha E_F}{E_g}\right)$$

with

$$E_F = E^0{}_F\left(1 + \frac{\alpha E^0{}_F}{E_G}\right)$$

and:

$$E^0{}_F = \left(\frac{h^2(3\pi^2 n)^{2/3}}{2m^*_e}\right)$$

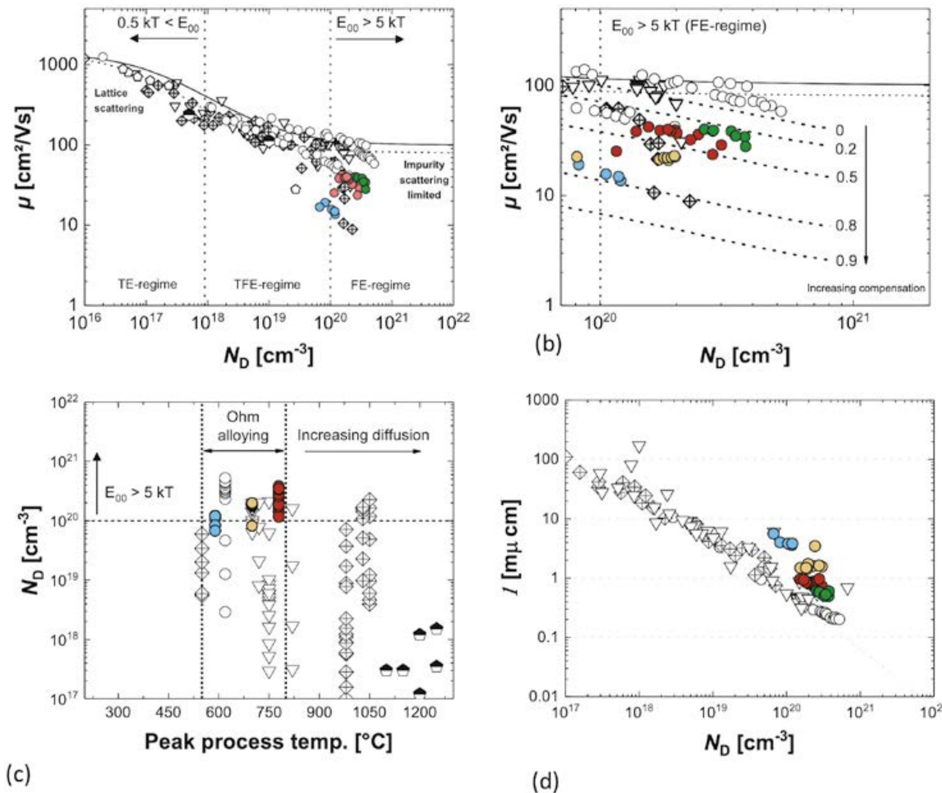


Figure 1: (a) Donor concentration vs. carrier mobility reported in literature for various growth methods: metalorganic chemical vapor deposition (quarters with cross); molecular beam epitaxy (diamonds); hydride vapor phase epitaxy (pentagons) reactive sputtering (grey circles); Si-implantation (half-filled hexagons). Samples in this work are colored: sample A (yellow); B (blue); C (red); D (green). Solid and dotted lines represent fitting from Schwierz et al. based Caughey-Thomas approximation; (b) N_D vs. μ in the range of $E_{00} > 5\,kT$. (c) Peak process temperature vs. measured donor concentration. Reported range of alloying temperatures of ohmic contacts to AlGaN/GaN are added as a reference; (d) carrier concentration vs. specific resistivity.

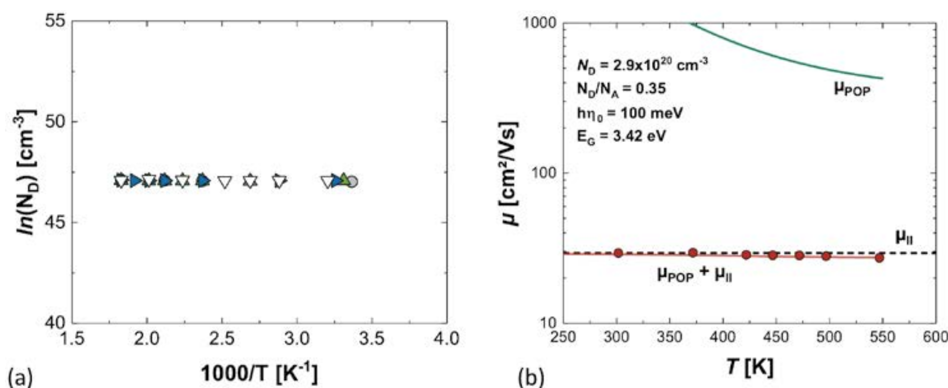


Figure 2: (a) Arrhenius plot of three different positions of sample C; (b) Temperature dependent electron mobility of the heavily doped GaN. Scattering by ionized impurities μ_{II} (black)b and polar optical-phonons μ (green) was modelled to fit the experimental data (red).

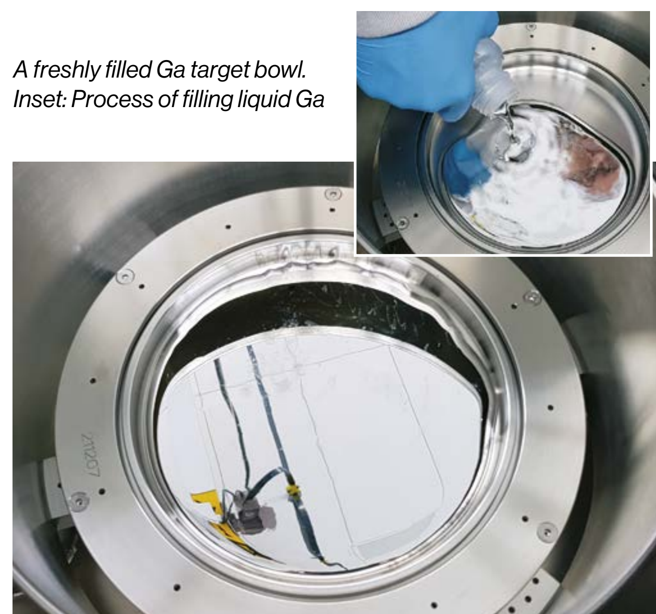
Where α (0.64) and m^*_e (0.22m_e) are the non-parabolic conduction band coefficient (α = 1(m^*_e/m_e))², and the electron effective mass, respectively. High carrier compensation ratios $\theta = N_D/N_A$ were found for MOCVD and MBE grown samples beyond $N_D > 1\times10^{20}$ cm^{-3} as shown in Figure 1b. In consequence, strong mobility decrease was reported limiting the achievable carrier density and specific resistivity. Compensation ratios of the co-sputtered thin films in this work were found to be rather constant up to $N_D = 3.7\times10^{20}$ cm^{-3} at higher growth temperatures. A significant increase in compensation ratio (is observed at lower growth temperatures (θ = 0.8), which could be attributed to a decrease in crystal quality where e.g., increasing amount of point defects (e.g., Ga-vacancies). The assumption is consistent with the increase in FWHM and decrease in peak intensity of the second 00.2-reflex observed by XRD. Only reactively sputtered thin films on 2-inch substrates from solid Ga-targets were reported with even higher carrier mobilities in the same range of carrier densities so far. Reported data are even higher than the impurity scattering limit at θ = 0, which was stated to be the result of an underestimation of the effective electron mass but not further discussed. Specific resistivity was derived and compared to reported data from the literature (Figure 2). Lowest specific resistivities in this work were obtained for highest growth temperature (800°C) with $\rho < 0.5$ mΩcm which is close to best reported values in literature independent of the growth method. An increase of resistivity is observed by lowering the growth temperature as a result of the increasing compensation ratio described before. Lowest resistivity of sample A (590°C) was found to be 3.5 mΩcm. The measured carrier concentrations are well beyond the theoretically, required doping to achieve a metallic character. To verify Mott-transition of the sputtered GaN films, temperature-dependent Hall measurements were carried out for T = 300 to 575 K. No significant change in electron concentration or electron mobility was observed within the measured temperature range indicating the degenerate nature of the Si-doped GaN films. Temperature-dependent polar optical-phonon scattering was modelled via:

$$\mu_{POP} = \frac{\varepsilon_0 \varepsilon_r \hbar}{eNm^*_F} \sqrt{\frac{\hbar}{2m^*_F \omega_0 (1 + \hbar\omega_0 / E_G)}} \left(1 - 5\frac{k_B T}{E_G}\right)$$

where $\hbar\omega_0$ is the optical phonon energy (100 meV). Scattering at dislocations is neglected since their impact on transverse mobility above $N_D > 1\times10^{20}$ cm^{-3} for dislocation densities below $N_{DISL} < 1\times10^{11}$ cm^{-2} is not relevant. Dislocation densities of MOCVD-grown GaN on sapphire with AlN nucleation layer (templates used in this work) are generally found to be lower much lower and the interface of sputtered GaN on MOCVD-GaN is not expected to generate new dislocations. Scattering at grain boundaries could be assumed for sputtered GaN, however, the associated potential barriers would lead to a thermal activation of the carrier mobility or carrier density. In addition, at high doping levels, most of the grain boundary related trap states are filled and the potential barriers would decrease in height and width. Temperature dependent fitting of the carrier mobility was achieved using Equation 2 and 7 by Matthiessens rule given in Figure 2b. Only minor contribution of μ_{POP} was found while μ_{II} clearly dominates the overall low-field scattering in the samples.

In conclusion, heavily doped GaN thin films prepared by co-sputtering from a liquid GaN-target were demonstrated. Extremely high donor concentrations above 3×10^{20} cm^{-3} at low process temperatures (< 800 °C) with specific resistivities below 0.5 mΩcm were achieved. Mott-transition was verified via temperature-dependent Hall-measurements revealing neither a change in mobility nor carrier concentration in the range of 300 to 550 K. Impurity scattering was determined to be the major low-field mobility limiting factor with a minor contribution of polar optical-phonon scattering at elevated temperatures. Scattering at dislocations or grain boundaries was ruled out to impact the total mobility. The results demonstrate the huge potential of sputtering as an alternative route for low-temperature, high throughout and easy upscaling of regrown n-type GaN.

A freshly filled Ga target bowl. Inset: Process of filling liquid Ga



HEXAGON Throwing a double in power device applications

Evatec's CLUSTERLINE® family of 200 and 300mm have a worldwide reputation as flexible, secure production solutions across a wide range of front and backside processes in power applications. But we like to stay ahead of the game especially when it comes to driving down cost of ownership. Read on as Product Marketing Manager, ***Fabian Kramer*** & Senior Process Engineer, ***Gerald Feistritzer*** give us an idea how HEXAGON could double your throughput in selected power device applications.

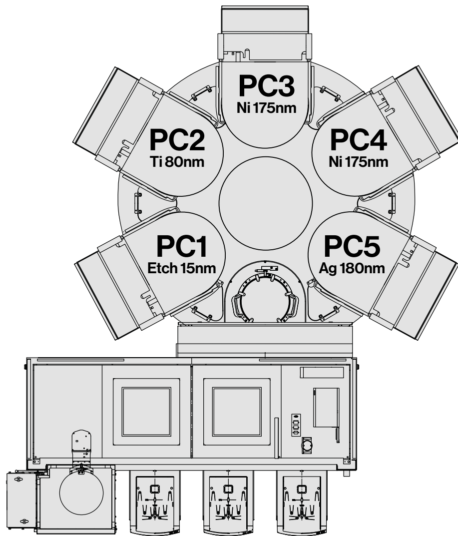
The challenge

Backside metallization has always been a sensitive market when it comes to cost of ownership. Evatec has been delivering solutions on silicon using CLUSTERLINE® for many years where secure thin wafer handling and management of stress are vital for the best process reliability and wafer yields. The market for applications using wide band gap (WBG) materials is also now developing strongly, so it's time to look at how we can help our customers develop the best production solutions for devices based on these new materials.

The new generation HEXAGON is already also known by many of our customers for delivering industry leading throughput and process performance in Advanced Packaging applications like FOWLP. Its "inline" configuration offering high speed wafer transfer and fast pumping offers a new approach for increasing throughput and driving down cost of ownership in selected power applications too, so lets take a look at some typical examples for processes for bonded or unbonded SiC wafers.

Case study 1: Thin SiC wafer – direct handling without carrier

Tool configuration

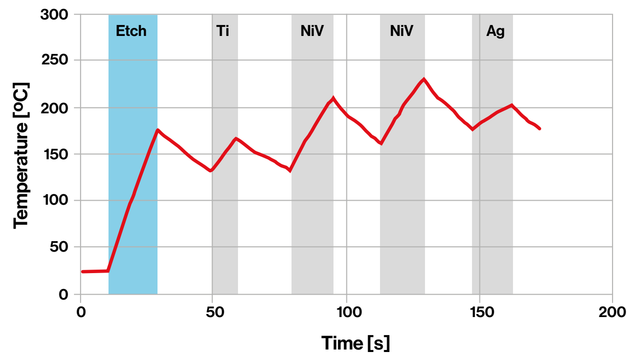


Results

Throughputs of up to 80 wafer per hour could be achieved. This is thanks to the short transfer times, rapid pump down, gas stabilization and pump clean steps inherent in HEXAGON architecture. Processing temperatures are also within the normal range compared with conventional processing on CLUSTERLINE®.

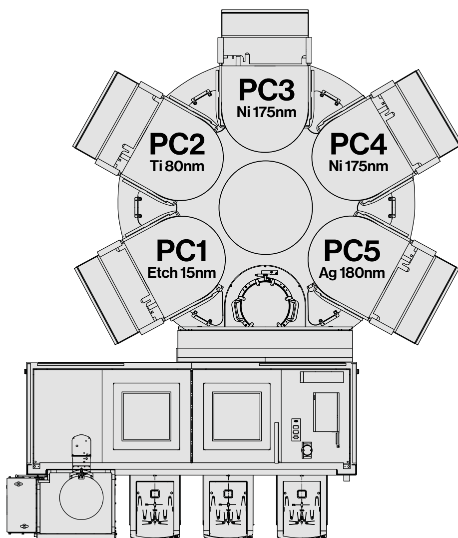
Assumptions

- Etch 15nm / Ti 80nm / NiV 350nm / Ag 180nm
- Thin SiC 250µm
- No T-limit



Case study 2: Thin SiC wafer bonded on glass carrier

Tool configuration

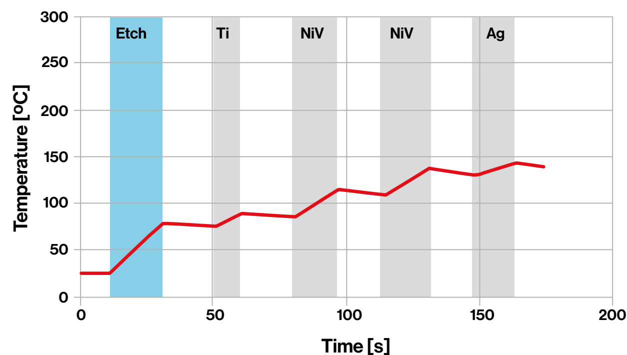


Results

Just like the first case study, the short transfer, pump down, stabilization and pump clean times give HEXAGON an immediate advantage but still enable process temperature to be controlled within the restricted range allowed for bonded wafers of 150ºC in this specific case. Throughputs >75 wafer per hour were achieved.

Assumptions:

- Etch 15nm / Ti 80nm / NiV 350nm / Ag 180nm
- Thin SiC 100µm bonded on glass carrier 900µm
- 150°C T-limit



HEXAGON – the solution for everything?

Of course not! CLUSTERLINE® along with its configuration for up to 6 cathodes, complete range of chuck options including clamping and reputation for the ultimate in temperature and therefore bow control still provides the most flexible solution in the market, but if HEXAGON can fulfill your process specs its undoubtedly a winning throw of the dice.

Find out if HEXAGON is the right tool for you

Our process team would love to talk to you and explore if HEXAGON could be the perfect fit for your application. Scan the QR code now to contact us to take the first step.