Enabling Robust SiC Power Device Fabrication with **Amorphous-Carbon Sputtering**

Evatec's Manager Process Development, **Gerald Feistritzer**, and Business & Technology Scouting Manager, **Dr. Vinoth Sundaramoorthy**, explain the motivation for using PVD processes for amorphous carbon (a-carbon) cap layers as a superior alternative to typical photoresist processes and report results for processes developed on CLUSTERLINE® 200. In addition to post-doping PVD deposition, a novel approach to pre-doping PVD deposition of the a-carbon layer was shown to be a potentially useful technique to modify the doping profile and downstream device performance.

Why Cap layers?

Silicon Carbide (SiC) materials have a wide band gap and high thermal conductivity compared to silicon materials, which makes them suitable in high-voltage applications. They can also be used for harsh environments (automotive, aerospace) where robustness and reliability of the semiconductor device are crucial. It is not easy to dope these materials using "diffusion", so they are typically "implanted" with high doses and at high energies to achieve source and drain regions of the silicon carbide power device.

Post-implantation annealing is then required to activate the dopants during SiC device fabrication, as the implanted dopants lie deep inside the bandgap. Annealing temperatures typically higher than 1600°C are used for dopant activation. During such high-temperature annealing, the surface of SiC substrates becomes very rough due to the out-diffusion of carbon atoms. This process, called "step bunching", causes surface degradation and affects the performance of the devices fabricated on these layers. In particular, the Metal-Oxide-Semiconductor (MOS) interface fabricated on these layers poses severe reliability issues. Hence, it is important to protect the SiC surface during the dopant activation annealing process.

Improving on existing CVD solutions

A thick carbon layer formed by depositing photoresist and annealing above 800 °C is typically used as surface protection during such a high-temperature activation process. However, this approach is not ideal for mass production with respect to both cleanliness and particle management, which might lead to yield issues in the fabricated devices. We have now been able to demonstrate that sputtering can serve as an effective alternative for the surface protection layer for SiC wafers.

Device Structure	Planar	Trench
Target - Substrate Distance	50mm	125mm
Typical film thickness (nm)	20 - 200	
WiW uniformity (%)	<5%	<15%
Typical deposition rate (nm/s)	1.5 - 1.7	0.6 - 0.8
Refractice index	2.3 - 2.4	
Typical film stress (MPa)	-800 to -400	

Figure 1a: Process performance data

- → System configuration: Single Process Modules (SPM)
- → Vacuum system: Cryo-pump
- → 6” or 8” chuck at room temperature
- → Shadow mask (full face deposition)
- → ARQ 151 DC sputtering 6kW, Ar sputter gas
- → Carbon target
- → Zoom shield

Figure 1b: Hardware configuration

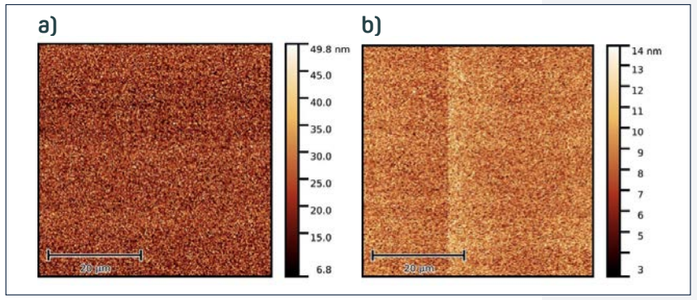

Figure 2: AFM analysis on samples with a) 20nm, b) 50 nm a-carbon layer. Both samples were annealed at 1800 °C.

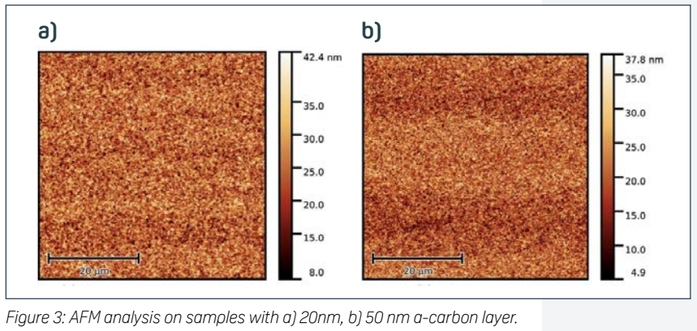

Figure 3: AFM analysis on samples with a) 20nm, b) 50 nm a-carbon layer. Both samples were annealed at 1900 °C.

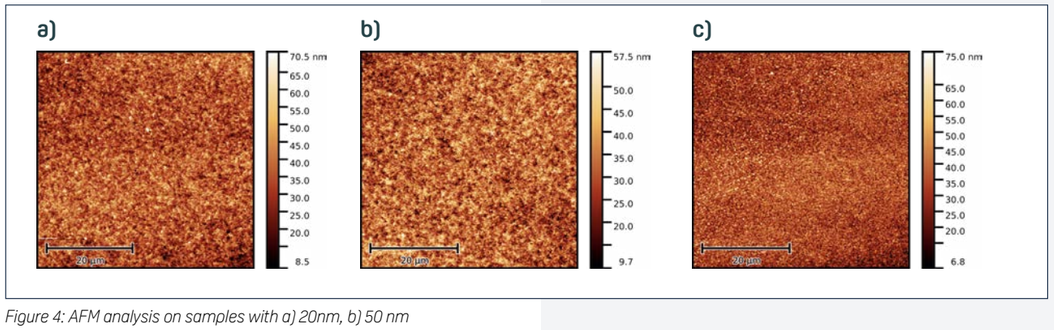

Figure 4: AFM analysis on samples with a) 20nm, b) 50 nm c) 280 nm a-carbon layer. All samples were annealed at 2000 °C.

Figures 2, 3, 4, 5 & 6 courtesy of Fondazione Bruno Kessler, Italy

PVD solutions on CLUSTERLINE® 200

Evatec’s advanced amorphous-carbon sputtering solution is specifically engineered for planar and trench power device applications. It enables high quality deposition using a single process module, streamlining production while ensuring exceptional uniformity and repeatability.
The hardware configuration, detailed in Figure 1b, delivers both flexibility and precision for demanding power device manufacturing environments.

Process results

To demonstrate the surface protection capability, a range of amorphous carbon layers were coated onto 6” 4H n-type SiC substrates with a thickness of 350 µm and a resistivity of 0.02Ωcm. The a-carbon layers were deposited using typical deposition conditions shown in Figure 1a.

Two thicknesses of amorphous-carbon layers were selected for the experiments: 20 nm and 50 nm. For comparison, a wafer with a carbon layer formed by photoresist and annealing was also analyzed. The wafers were annealed in a centrotherm c.ACTIVATOR 200 furnace at temperatures between 1800°C and 2000°C. To benchmark the performance of the photoresist-formed carbon layer, an equivalent thickness (280 nm) of PVD a-carbon layer was also deposited on SiC wafers. Finally, structural analysis was performed at partner Fondazione Bruno Kessler (FBK) in Italy.

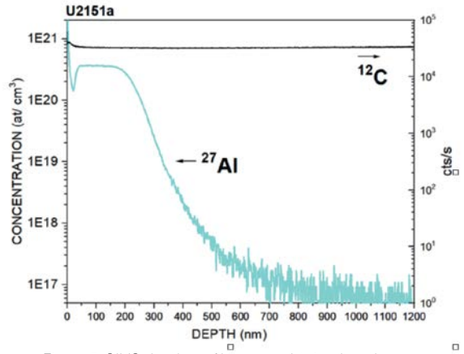

Figure 5: SIMS depth profiles were obtained on the sample implanted with Al species at 500°C. A 50 nm a-carbon layer was deposited before implantation.

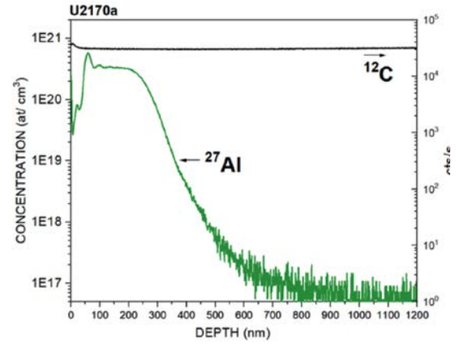

Figure 6: SIMS depth profiles were obtained on the sample implanted with Al species at 500°C. A 50 nm a-carbon layer was deposited after implantation.

	Temperature		
A-Carbon thickness (nm)	**1800°C**	**1900°C**	**2000°C**
20 nm	4.46 ± 0.42 nm	4.32 ± 0.26 nm	6.61 ± 0.53 nm
50 nm	2.12 ± 0.19 nm	4.18 ± 0.32 nm	6.49 ± 0.48 nm
280 nm	–	–	6.15 ± 0.47 nm

Table 1: Comparison of surface roughness for different a-carbon layer thickness until 2000°C annealing temperatures.

In Figures 2 and 3, we can see that sputtered PVD layers provide good protection of SiC surfaces up to 1900°C with a minimum layer thickness of 20 nm. It was also seen that the surface roughness decreases for SiC wafers with increasing amorphous-carbon protection layer thickness until 2000°C. For temperatures of 2000°C (Figure 4), 20 nm thick layers are not sufficient, but the properties improve with increasing layer thickness. The values of the surface roughness measured using Atomic Force Microscopy (AFM) are recorded in Table 1. It can be seen that the average surface roughness of the SiC surface decreases with increasing a-carbon layer thickness at all annealing temperatures until 2000°C. In general, a 50 nm a-carbon layer can protect the SiC surface against step-bunching until 1900°C, comparable with the performance of a-carbon layer formed from photoresist, and this is a very useful feature for making novel semiconductor devices like super-junction structures.

Modification of dopant profile in SiC layers

A-carbon was analyzed as a surface protection layer on the implanted samples to test its effectiveness in screening the defects that are generated during the implantation process. SiC wafers were implanted with Al or P species at different doses and energies to create a dopant profile. Again, two different a-carbon layers were deposited: 20 nm and 50 nm. An a-carbon layer was deposited on some wafers before implantation and some wafers after implantation to analyze the screening effectiveness. All implanted samples were annealed at 1750°C. SIMS profiles were performed on these implanted wafers to investigate the effectiveness of the a-carbon layer.

It can be seen from Figure 5 that a 50 nm a-carbon layer deposited before the implantation avoided the spike in carrier concentration on the surface of the SiC wafer. The peak carrier concentration of Al was 3.5E20 cm^{-3}.

Similarly, the peak carrier concentration of Al in the sample where a 50 nm a-carbon layer was deposited after the implantation process was 6E20 cm^{-3}, which was observed as a spike in the Al concentration (Figure 6). Hence, the doping profile of the implanted wafers can be altered with a thin a-carbon layer. This could be due to the fact that the a-carbon layer acts as screening layer in blocking peak concentration on the SiC surface and reduces the defects formed on SiC surface during the implantation process. This feature could be very helpful in modifying the implant profile and modulating the device performance.

These results enable novel design and support chip manufacturers to produce next generation SiC devices. Let’s talk some more about how we can support you and your own process innovations.