FRONTEND

300mm frontend integration

Reaching for the sky

As the semiconductor industry evolves, it continues to follow two key innovation paths: “More Moore”, focusing on continued transistor scaling and performance improvements, and “More than Moore”, targeting functional diversification through advanced packaging and integration of different technologies.

Admir Asanoski, Head of Business Field Semiconductor and Advanced Packaging, and **Kai Wenz**, Senior Program Manager Technology Development, explain how Evatec supports both strategies with new innovative solutions.

The move to smaller feature sizes is relentless

With 2D scaling reaching physical limits, new strategies such as 3D integration, novel materials, and innovative device architectures are essential to meet the demands for higher logic density and multifunctional system performance. These trends demand increasingly sophisticated thin-film deposition capabilities, enhanced contamination control, and improved process reliability. Figure 1 illustrates the big picture where capabilities required for both strategies come together to satisfy increasingly complex device needs.

CLUSTERLINE® 300 – Building on a strong foundation

Evatec set the baseline back in 2022 for its initial planar frontend capabilities by having the right hardware in place through its CLUSTERLINE® 300 platform. Since that time we have been focused on an extensive program in advanced directional sputtering (ADS) to enable small feature sizes and more complex architectures. Figure 2 illustrates the principle of how we build a final solution optimized for mass production in the market combining hardware and process know-how.

We can already offer qualified processes for frontend planar layers like Ti, TiN, Al alloys, Ta and TaN at very low particle levels and layers free of metallic contamination. We can now also support next generation materials e.g. Ruthenium. We are continuing on our road of process development offering Standard Directional Sputtering (SDS) for lower aspect ratios (AR) up to 5:1 and via and trench structures with critical dimensions (CD) >110nm suplemented by Advanced Directional Sputtering (ADS) for higher performance and aspect ratios up to the limit of PVD for via and trenches CD >35nm.

A choice of

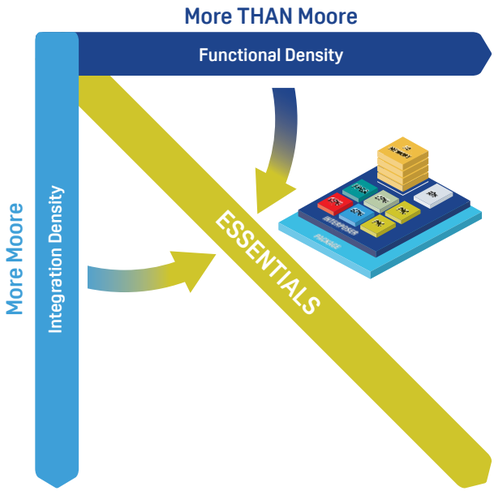


Figure 1: The Big Picture: Innovations for future essential chips.

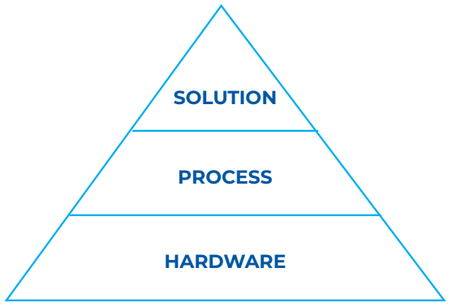


Figure 2: CLUSTERLINE® 300 – a strong foundation on which to build customer solutions.

Items	Conventional	High-End	
		Standard (SDS)	Advanced (ADS)
KEY FEATURES:			
HOT/COLD ESC			
SHUTTER			
			
WiW RS/THK uniformity	<5%	<3%	<3%
Target-Subtrate Distance	short	short /mid	long
Structures	Planar, Reflow	CD >110nm /AR 5:1	CD >35nm
Shutter	Yes	Yes	Yes
300mm hot/cold ESC	Yes	Yes	Yes
DC Sputter power	DC	DC	DC
	DC pulse	DC pulse	DC pulse
RF chuck bias	Yes	Yes	Yes

Figure 3: A range of solutions according to application demands.

CLUSTERLINE® 300 process modules

The current solutions available can be split into “conventional” and “high-end” frontend (see Figure 3). The conventional setup is focused on the best target utilization using long-life targets beneficial for thicker layers, whilst high-end solutions for thin layers are tuned for performance for each application.

In all cases, however, configurations are equipped with the same common capabilities such as shutters for cleaning and chamber preparation, hot/cold electrostatic chucks for full temperature control with full-face deposition, and supported by additional frontend reoptimized ICP etch chambers with H_2 capabilities, and high pressure degas and cool chambers.

Besides good WiW and WtW uniformity, the SDS solution can also deliver via nanostructures up to 5:1 AR with good step coverage performance (Figure 4). Further enhancement of performance will come with an ADS solution. Performance for trenches is typically even better by minimum factor of 1.5 compared to vias.

Mechanical particle levels can be controlled typically to levels in the range <20adders for sizes >60nm with metallic contamination controlled to <1.0E+10at/cm² for the standard frontend materials.

Productivity depends on the process flow. It can reach up to 50wph on a fully-equipped next generation CLUSTERLINE® 300 platform for TiAl deposition for memory applications. It achieves a barrier for Al through a 10nm thin Ti layer with excellent surface quality that avoids spiking into the silicon through full process control of our electrostatic chucks, pre- and post-treatments (Figure 5).

For different applications such as high bandwidth memory this Al layer can be temperature stress stable to achieve wafer bow always below <200µm.

We have in-house sampling capabilities for Ti, TiN, Al-alloys, Ta, TaN, and Cu including pre- and post-treatment like high pressure degas, cool, and ICP Etch (Ar and/or H_2). In-house metrology techniques include sheet resistance, thickness, particles, XRD, SEM /FIB, reflectivity (see Figure 6). Please also ask us about other materials for processing in basic and SDS module configuration.

There are many more exciting developments still to come on 300mm. Knowing that this is not the end, we already plan our next steps by adding the CVD and ALD capabilities that exist already on our 200mm platform to CLUSTERLINE® 300 too e.g. for high-end directional sputtering (HDS) and nanostructures <35nm where PVD on its own will no longer be sufficient. You can also read more about our ALD developments on page 26 in this year’s LAYERS.

The new developments for ADS and beyond will also include the development of a new cluster platform that will allow more single process chambers to be added to one platform fulfilling the solution needs that are planning to be released together with the final ADS solution. All these new developments will bring Evatec to the next level as a semiconductor solution provider, preparing for a future where we really can reach out for the sky together with our customers.

If you would like to learn more about what we are doing including accessing the capabilities within our ECL process laboratory, please “reach out” too! Simply contact your local Evatec service organization.

Structure dimensions	Diameter 110nm Depth 450nm	Diameter 160nm Depth 450nm	Diameter 250nm Depth 450nm
	Average %	Average %	Average %
Top Sidewall	19%	46%	43%
Middle Sidewall	10%	32%	27%
Low Sidewall	10%	33%	29%
Bottom	32%	17%	28%

Figure 4: SDS Step coverage performance.

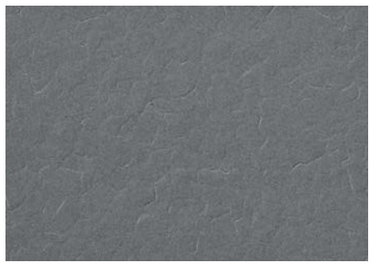
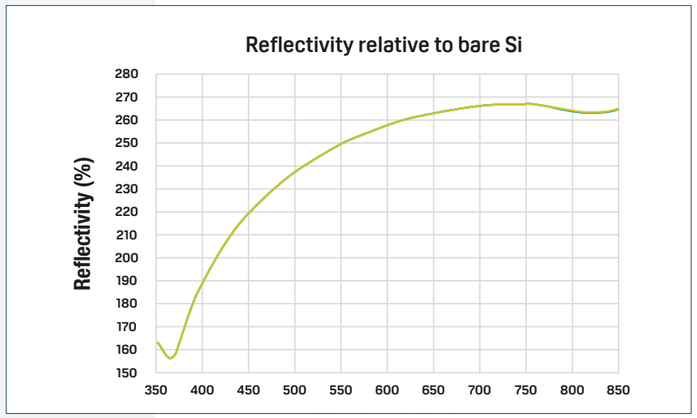


Figure 5: Excellent TiAl layer surface quality



Reflectivity refer to Si @436nm	Result
Center	212%
Edge	212%
Range	0.05%

Figure 6: Reflectivity performance of TiAl layer