# IMPROVING PRODUCTIVITY AND YIELD IN SEMICONDUCTOR POWER DEVICE MANUFACTURING

Evatec's Product Marketing Managers **Hans Auer** and **Gernot Engstler** give us an overview on the state of play in front and backside metallization processes and production solutions on CLUSTERLINE®

## Market requirements

Power devices, or more specifically "solid state electrical devices" are used to control electric power.

Silicon semiconductors have been employed in power circuits since the invention of the solid state diode by William Shockley in 1960. Today the discrete power device market has achieved a size of nearly 20 billion USD with a predicted CAGR of ~7%. This continuous growth is driven by the ever-increasing needs for energy management and control in domestic and industrial markets, mobile communication/computing and most recently by greenhouse gas reduction initiatives. Electric vehicles like cars and trains as well as renewable energy generation looks set to spur the major part of power device development and growth.

The move from 200 mm/8" to 300 mm/12" Si wafers is driven by the need to reduce production cost and fulfill increasing market demand. Scaling up manufacturing to 300 mm requires production tools with specific capabilities. A large part of the innovation for next generation power transistors is taking place within wide bandgap GaN and SiC technologies, with new systems design and processes.

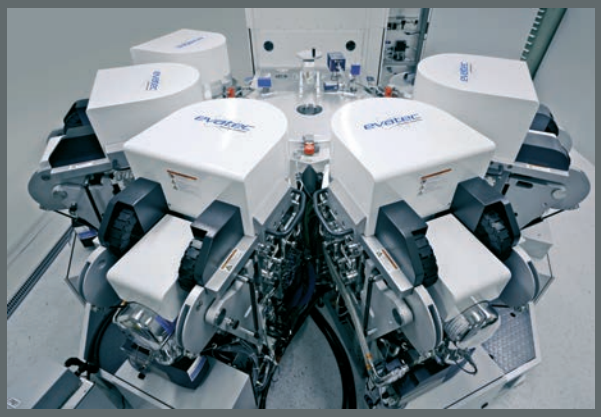
The wafer is a functional part of the device and needs to be processed on both sides. Metal deposition processes create the essential components of the device: source, gate and drain. For backside metallization the system design and process must be optimized for thin wafers. To minimize wafer bow, the stress introduced by the metal layer stack must be minimized. The wafers need to be handled and processed without any frontside contact to avoid damage. Frontside processing requires deposition of thick metal, typically aluminum alloy, which needs to be produced at high deposition rates for reasons of productivity.

## Evatec capabilities

Evatec has a strong footprint in the power electronics sector, both as the industry leader in metallization of traditional power devices and now for latest generation MOSFET and IGBT devices with very thin Si wafers of both 200 mm/8" and 300 mm/12". Evatec's know-how and dedicated solutions for frontside and backside metallization on CLUSTERLINE® helps give our customers competitive advantage.

Current state of the art technology includes fully automated handling and processing platforms for Si wafers and SiC substrates with high equipment uptimes and device yields. Delivering solutions to deposit stress sensitive 4-layer backside metal stacks with integrated "in-situ" clean & etch for oxide removal and annealing capability for the ohmic contact formation is just part of our daily work.

Experience in silicon power devices and in related technologies such as GaAs III-V devices or GaN technology from the LED industry mean we are ideally positioned to help our customers develop and industrialize these new innovative power device types.



*CLUSTERLINE® 300*

# Solutions for frontside metallization

The frontside of the wafer requires deposition of a thick metal layer, typically 5 microns or more of aluminum alloy (AlSi or AlSiCu). Uniform coverage e.g. >50% in contact openings needs to be provided for sufficient metal coverage to conduct the high currents. Uniform coverage across the entire wafer is key to device yield and reliability.

## Al alloy (AlSi, AlSiCu) deposition on Si

A good and uniform step coverage in the contact structures across the entire wafer requires equally uniform Al vapor approach angle profiles across the entire wafer surface. This is accomplished by optimizing the target erosion profile.

Depositing Al alloys on Si further requires the process temperature to be stable and limited to <350°C. This enables control of grain size and avoids Si precipitation.

The graphs in figures 1a and 1b demonstrate the benefits of effective temperature control for a 5 micron thick AlSi film. Temperature during deposition was measured with an in-situ pyrometer directed at the wafer surface.

An electrostatic heat chuck (hot ESC) was used in the production of this data, where the wafer has a full-face contact to the chuck and the thermal coupling between chuck and wafer can be effectively increased by applying backside gas. The tight interface between wafer and ESC allows backgas pressures of up to 5 mbar, helping to further improve the coupling. The ESC configuration is the superior solution to ensure, that the energy introduced by the PVD process is dissipated to the chuck. The resulting temperature stability provides the basis for highly reproducible film properties.

The resistivity data is indicated in figure 1b and demonstrates the benefit of an ESC for optimum temperature control of the film. Stabilizing the wafer temperature at approximately 350°C results in lowest film resistivity.

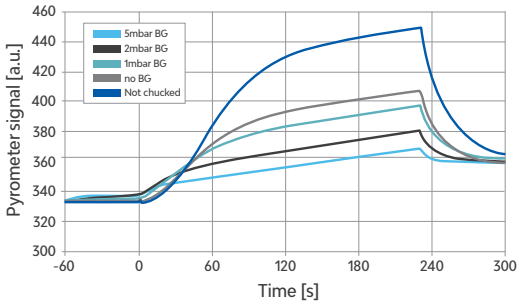



*Figure 1a.*

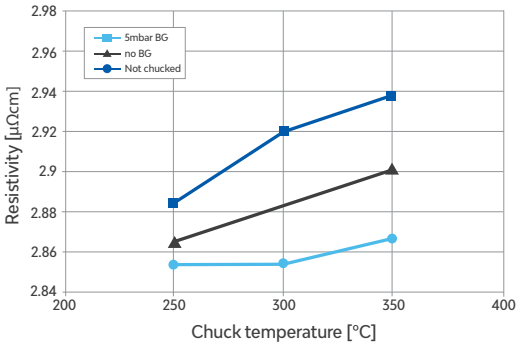



*Figure 1b.*

For reasons of high productivity, high deposition rates of between 1 and 1.5 microns/min are required. The challenge is to apply high powers of up to 40 kW (300mm wafers) at stable process temperatures. A well defined process window with strict control of process temperatures and high deposition rates requires excellent thermal coupling between chuck and wafer. Clampless chucks or electrostatic chucks (ESC) combined with a dedicated process kit (e.g. shield design) provide thermal stability and reproducibility resulting in optimum Al film uniformity and step coverage.

Rotating planar magnetron technology with long-life targets and high target utilization optimized for uniform step coverage provides an ideal solution.

## Ti/TiN liner/barrier for trench contacts

Power devices with reduced form factor and footprint call for optimum contact properties, whilst the conservation of energy demands the reduction of electrical losses in modern switching devices. Trench contacts have become more and more common to provide low contact resistance. Their formation requires barrier films with high conformality and an efficient hot Al flow process to entirely fill the trenches.

Conformal Ti/TiN barrier films can be realized by Highly Ionized Sputtering (HIS), a technology where material is deposited at high energy levels, and deposition is focused in the vertical orientation of the device structure. The sputtered atoms are ionized in a high density plasma and directed to the wafer. The high plasma density produces a very high degree of Ti ionization of up to 50%. Figure 2 shows the relationship between plasma density, discharge current and Ti ionization as measured by Atomic Absorption Spectroscopy.

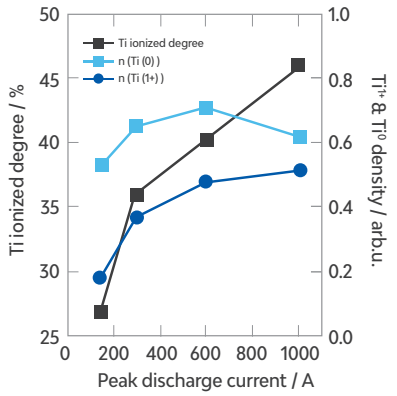



*Figure 2.*

Back-sputtering by RF Bias (figure 3) further improves the side wall coverage in the trenches. In comparison with DC sputtering bottom and sidewall coverage for Ti/TiN barrier layers can be increased with HIS by a factor 2 to 3. For example, for a trench with aspect ratio of 2:1, a bottom coverage of 80% and sidewall coverage of up to 15% was achieved.

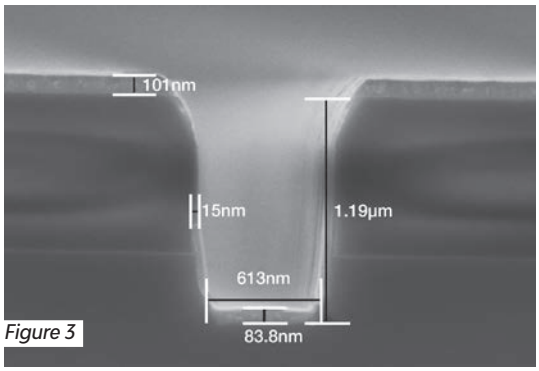



*Figure 3*

HIS not only features directional deposition for improved conformality but also the fine grained and dense films required for superior barriers. Traditionally DC sputtering has been combined with RF Bias because of the positive effects on film grain size and density. The results in 4a-c show the outstanding performance of HIS in direct comparison with DC sputtering.

These latest advancements in PVD technologies deliver optimum trench contact capabilities and provide the basis for even smaller device structures.

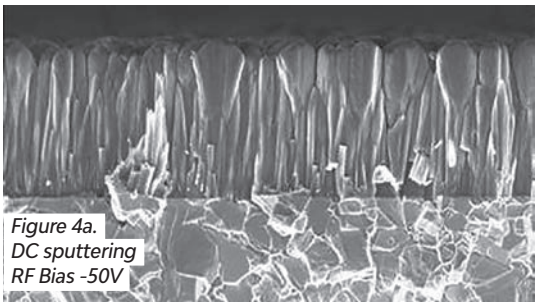


*Figure 4a.*
*DC sputtering*
*RF Bias -50V*

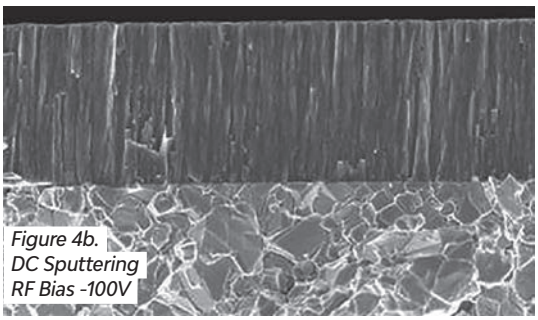


*Figure 4b.*
*DC Sputtering*
*RF Bias -100V*

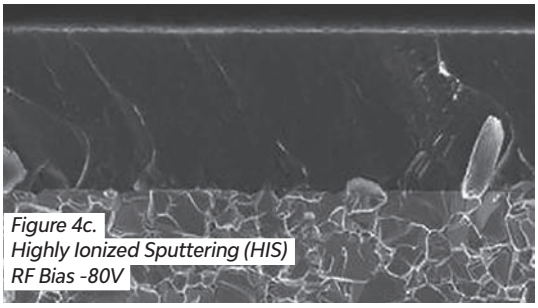


*Figure 4c.*
*Highly Ionized Sputtering (HIS)*
*RF Bias -80V*

## Hot Al flow for trench filling – flowed Al

Al fill (figure 5) requires high, stable and uniform wafer temperature, typically around 430°C, to ensure an efficient Al flow into trenches. ESCs or clampless chucks with temperatures of 500°C or even higher provide the required process conditions. A dedicated process flow has been developed for the thin seed layer deposited at moderate temperature and is followed by the actual fill process providing the uniform filling of the trench. Finally, a bulk layer is deposited at high sputtering rates to provide the required total film thickness.

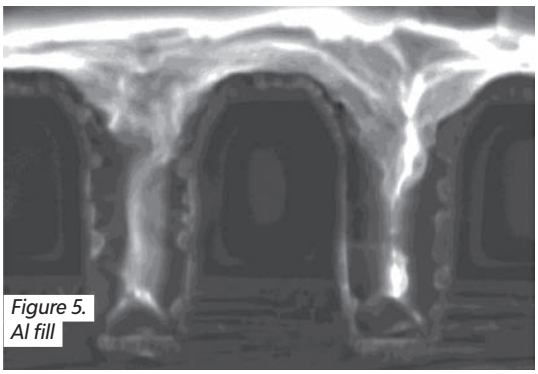


*Figure 5.*
*Al fill*

### Cost of ownership

A low cost of ownership requires long-life consumables: The ARQ sputtering source for 300mm wafers is equipped with a 25 mm thick aluminum target providing a lifetime of 3500 kWh with Rs uniformity <1.5% across target life. This equates to up to 6000 microns of materials deposited on wafers.

The process kit is optimized for a shield lifetime that lasts for the entire target life. Consequently, scheduled maintenance is only required together with the target exchange. This results in higher system availability and lower cost for kit cleaning. These new combined capabilities feature significantly reduced cost of ownership and cost of consumables.

### Summary

Optimum trench contact capabilities for barriers to form metal contacts require high conformality of Ti/TiN barriers with bottom coverage greater than 40% (aspect ratio of up to 4:1) and an optimized process flow for hot Al fill process. To fulfill the requirements of depositing thick films for Al bulk layers, the process equipment needs to be optimized for high deposition rates and perfect temperature stability.

CLUSTERLINE® provides high productivity metal deposition solutions for frontside metallization with tight control over film thickness, process temperature, bottom coverage and conformality which are key to device yield and reliability.

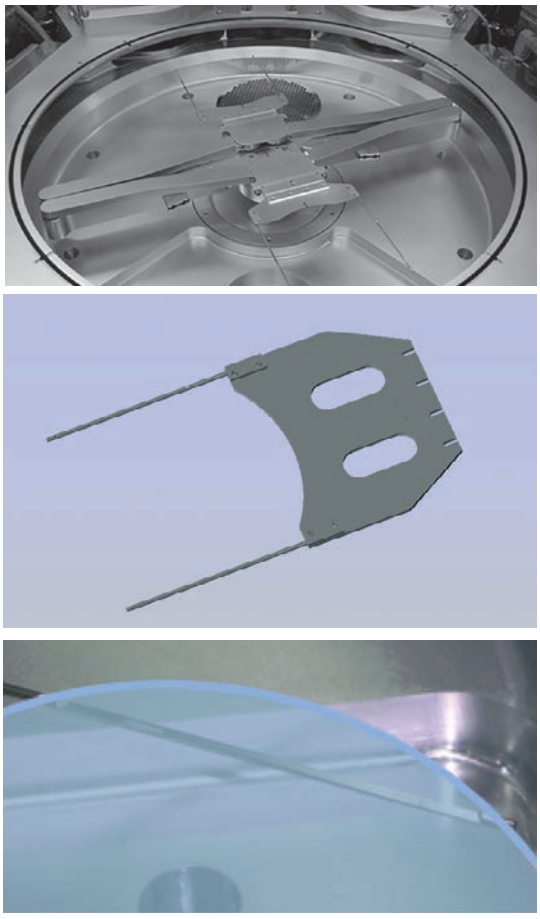
## Solutions for backside metallization

Power devices require backside metallization to provide good electrical and thermal contacts, and good adhesion between layer stack and the Si wafer are essential. The quality of this layer stack significantly contributes to the reliability of operation in the lifetime of the device.

It typically consists of aluminum (Al or AlSi), nickel (Ni) or nickel vanadium (NiV), and silver (Ag) or gold (Au). Since wafers are thinned prior to backside metallization, this is a critical application with demanding requirements. Backside processing requires the wafers to be handled and processed without any frontside contact to avoid damage and contamination of the wafer frontside. For backside metallization the system design and process must be optimized for thin wafers. CLUSTERLINE® equipped for backside metallization is prepared specifically to fulfill these requirements.

### Wafer handling

Edge contact for wafer handling and alignment as well as recessed chucks to hold the wafers during deposition are just two of the various features ensuring safe and reliable backside processing. Thin 300 mm and Taiko wafers with a maximum bow of up to 6 mm are typical standards.



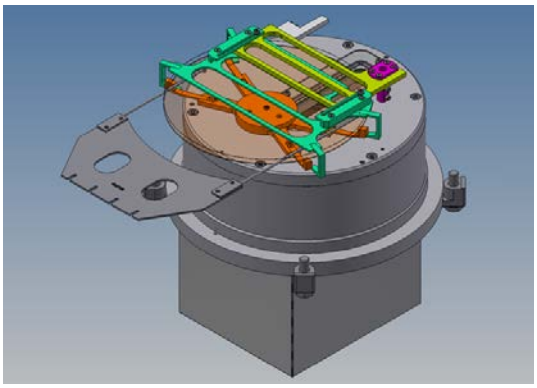
A vacuum robot equipped with rod end effectors featuring edge support and centering improves handling reliability and prevents damage of the wafer frontside. This design is proven in production on an installed base of more than 70 CLUSTERLINE® backside metallization systems worldwide.

### Wafer mapping and alignment

Thin wafers and Taiko wafers each require dedicated solutions for reliable wafer mapping in the cassette. Typically, wafer cassettes with higher spacing are used. In some cases metal cassettes with 13 slots with better clearance of robot and end effector offer a more reliable solution.

To align the wafer's lateral offset and the rotational notch or flat orientation without touching the device surface area, a sophisticated optical Edge Contact Aligner is applied. During the entire alignment procedure, the wafer frontside is exclusively touched at the edge, preventing any contact to the device zone.

## Processing



Prior to backside metallization wafers are thinned because the substrate is a functional part of the device. 300 mm/12" wafers are either reduced to a thickness of ~ 200 microns or the so-called Taiko-wafer grinding principle is followed. In the latter case the Si wafer consists of an outer Taiko-ring with a thinned Si membrane. For 300mm/12" wafers this membrane is thinned to 60, 90 or 120 microns depending on the device voltage class. The low thermal capacity of the thin substrate requires stringent control of the process temperature. The temperature during deposition has a significant impact on intrinsic film stress. To minimize wafer bow, the stress introduced by the metal layer stack must be minimized. CLUSTERLINE® features special chuck designs to control wafer temperature without frontside damage. In standard applications a recessed chuck configuration is used. In this classic design the wafer resides on an outer ring during deposition, preventing any contact to the device surface. However, whilst the recessed chuck is a cost-effective solution, thermal coupling is limited due to the lack of active chucking. Therefore, for applications requiring more stringent temperature control, a unique BSM-ESC (electrostatic chuck for backside metallization) is preferred.

## Degas and ICP etch

Prior to deposition, a degas and ICP etch step is included to reduce contamination, remove native oxide and create a shiny metal film. This in-situ pre-treatment contributes to the improved adhesion of the layer stack and the contact resistance.

A dedicated BSM degasser is required in the case of wafers carrying volatile species e.g. through organic passivation on the wafer frontside. Rather than using traditional designs with halogen lamps, the BSM degasser integrates an IR-heater with significantly improved temperature control and stability in production. Temperature measurement by pyrometer ensures reproducible process conditions and prevents overheating of the wafers. The degasser is integrated in one of three treatment stations located in the VTM (vacuum transfer module) and does not occupy a port for the SPM (sputter process modules). This configuration improves throughput and reduces cost of ownership.

An in-situ ICP Soft-Etch is used to remove the native oxide with minimal damage to crystal structure of the wafer. Such oxide removal is required for a low ohmic contact of the metal layer to the wafer. An in-situ annealing step can also be added if required.

## Typical backside metal layer stack

The typical layer stack for backside metallization (figure 6) consists of Al, forming the contact to the Si wafer, Ti as a barrier layer, Ni or NiV as the wetable layer for soldering and an Ag or Au top coating to protect the NiV from oxidation.

Critical for high yield and reliability of the power device are the good adhesion and low contact resistance of the Al or Ti contact as well as low stress introduced by the NiV layer.

## Al contact formation

The formation of a good ohmic contact between Si wafer and Al layer not only requires a Si surface that is clean and free of damage, but also a well controlled process temperature to enable the required Silicon-Aluminum reaction. Figure 7b indicates the desired result, the AlSi reaction called "spiking" required to produce a good ohmic contact.

| Process Step | Etch | 1st Layer | 2nd Layer | 3rd Layer | 4th Layer | |
|---|---|---|---|---|---|---|
| Material | $SiO_2$ | Ai | Ti | NiV | Ag | Au |
| Layer properties | | | | | | |
| 1. Thickness (nm) | | 200 | 100 | 200 | 600 | 200 |
| 2. Thickness uniformity (± %) | | < 3.5 | < 3.5 | < 3.5 | < 3.5 | < 3.5 |
| 3. Reproducibility (W to W ± %) | | < 2 | < 2 | < 2 | < 2 | < 2 |
| 4. Deposition rate (nm/s) | | up to 20 | up to 8 | up to 8 | up to 40 | up to 8 |
| 5. Stress (MPa) | | < 250 | < 400 | < 400 | < 300 | < 150 |
| 6. Resistivity (µOhm*cm) | | < 3 | < 70 | < 60 | < 3 | < 4.5 |

*Figure 6.*

Spiking is an effect where the aluminum starts to consume some of the silicon from the wafer. This process needs to be controlled, since insufficient spiking results in a bad contact, while excess of spiking can create damage to the wafer and affect device reliability. The use of Al alloy doped with approximately 1% of Si further helps to control the reaction. Since the reaction is highly temperature dependent, process temperatures need to be well managed. A temperature of 300°C to 350°C provides the optimum results. This temperature can be achieved by optimizing the energy introduced to the wafer during metal deposition of the Al layer or one of the following process steps, e.g. NiV.

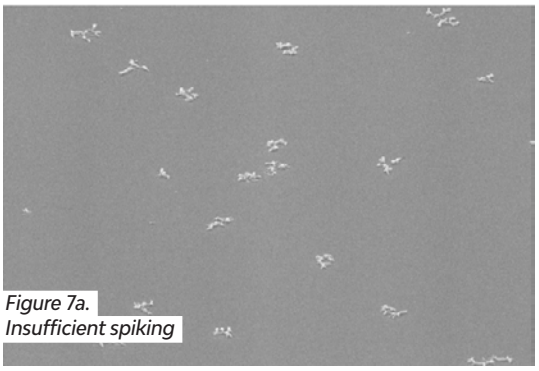


*Figure 7a.*
*Insufficient spiking*

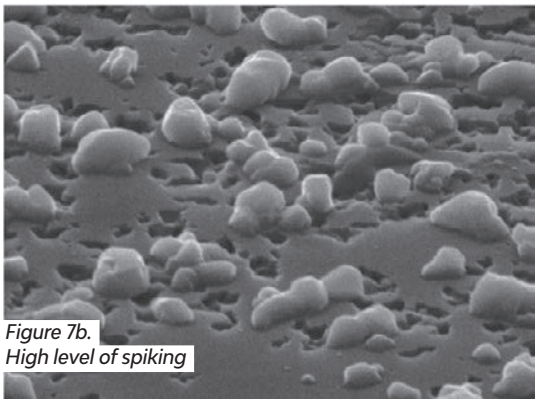
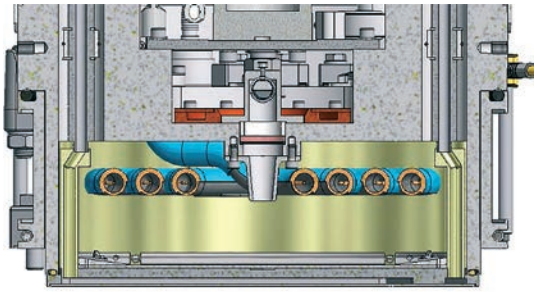


*Figure 7b.*
*High level of spiking*

CLUSTERLINE® provides two solutions for in-situ annealing shown in figs 8a & 8b.

Best results can be achieved by adding an annealing step in a dedicated process station. This allows high temperatures for contact formation independent of individual layer thicknesses and directly after deposition of the Al-contact layer. The PVD process can be optimized for minimal stress and wafer bow, e.g. by low temperature film deposition, since the contact formation is controlled individually in the consecutive annealing process.

**Anneal Module**



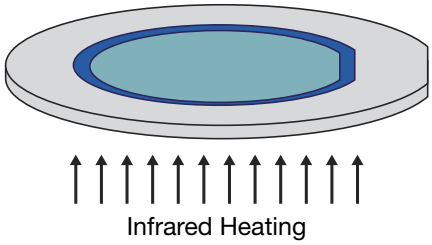
**System integration**
- Treatment station in VTM

**Basic Principle**
- Top side heating by lamp or IR heater with pyrometer monitoring

**Advantages**
- Direct heating of metal layer after Al deposition
- Independent of PVD process

*Figure 8a.*

**IR Heater Chuck**




**System integration**
- Chuck in PVD process module

**Basic Principle**
- Bottom side heating by IR heater element embedded in chuck

**Advantages**
- No extra process module needed, e.g. integrated in Al PVD module

*Figure 8b.*

## NiV layer and wafer bow

Stress is tunable for most materials. In the backside metallization layer stack the nickel (Ni) or nickel vanadium (NiV) solder layer introduces the highest stress compared with all the other metals. The intrinsic stress of the solder layer needs to be reduced to prevent high additional wafer bow after deposition and to ensure high device yield and reliability in operation.

Relative to Ni, NiV offers the advantage that stress can be controlled through several tuning parameters. Many manufacturers who have traditionally used Ni evaporation processes have therefore shifted to NiV when moving to sputter. Sputter provides superior performance since additional process parameters are available to control and optimize the critical film properties.

A film deposited by evaporation (figure 10a) is typically quite disordered and clustered, whereas sputtering (figure 10b) offers more uniform structured layers.

In general terms sputtering simplifies the process flow and improves reproducibility by safe pre-clean (degassing, etching) in-situ and under vacuum. The automation of wafer handling and processing is easier than for evaporation reducing the risk of human errors, and minimizing wafer breakage, contamination and yield loss.

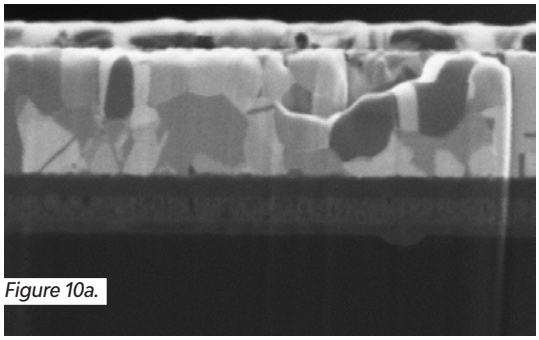


*Figure 10a.*

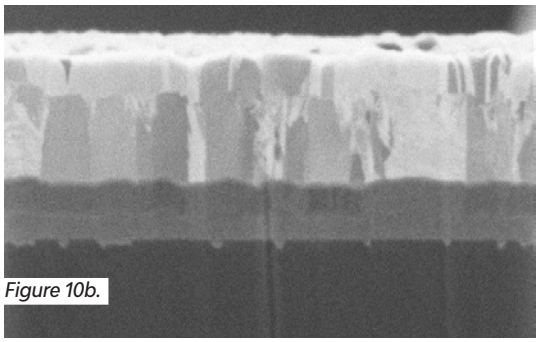


*Figure 10b.*

High temperature during deposition creates tensile thermal stress after cool-down, so it is important to minimize the thermal energy introduced during NiV deposition. This can be achieved by introducing several individual deposition steps and allow cool-down phases in between or by improving the thermal contact between wafer and chuck. CLUSTERLINE® uses conventional chucks with high heat transfer or ESC to stabilize wafer temperature during deposition. Another effective method is to produce a higher energy impact on the film, e.g. low pressure or pulsed DC. Both drive the stress towards compressive and compensate for the tensile stress induced by temperature. Figure 11a demonstrates the effectiveness of the different tuning parameters for a 550 nm NiV layer.

An optimized process for an Al / Ti / NiV / Ag layer stack results in an additional bow of less than 20 microns. Using all tuning parameters, it is possible to reduce the delta bow to zero. These results were generated on a CLUSTERLINE® system running 130 micron Taiko wafers and a NiV layer thickness of up to 1100 microns (figure 11b).

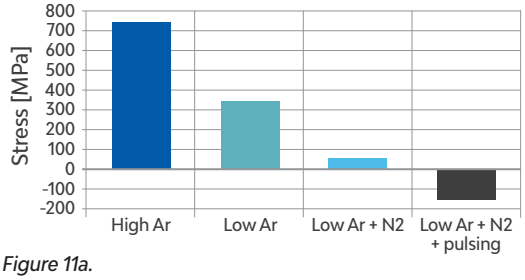



*Figure 11a.*

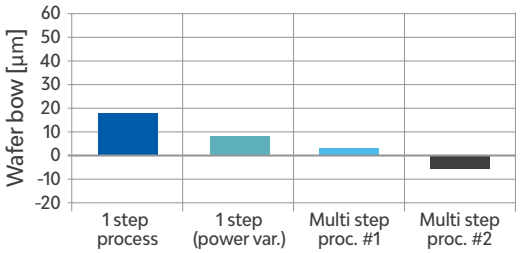



*Figure 11b.*

## Summary

The reliable handling and optimum processing of thin wafers and Taiko wafers requires a dedicated system and process. Reliable and defect free wafer handling, stress optimized processes and stringent temperature control are required for reliable wafer processing at high productivity, e.g. throughput and yield and to minimize cost of ownership.

Good ohmic contact formation, adhesion and minimal wafer bow (low film stress) are the critical properties for device performance, reliability and yield. Effective backside metallization processes allow the tuning and optimization of process parameters in a way that results in best device properties.