Innovations and Opportunities

in Panel Level Packaging

Things are moving fast in the world of Panel Level Packaging. **Mohamed Elghazzali**, Manager Technology Development, **Stanley Low**, Product Marketing Manager, and **Admir Asanoski**, Head of Semiconductor & Advanced Packaging, expand on Evatec strategy and roadmaps, making sure our market offerings can address the full spectrum of customer requirements.

Advanced Panel Level packaging enables higher bandwidth and improved thermal management, both of which are critical for AI chiplets. Moving from Wafer Level Packaging (300 mm wafers) to panel formats such as 310x310 mm, and extending solutions to larger areas up to 650x650 mm, is part of the evolution that Evatec is ready to enable with its platforms.

Evatec's CLUSTERLINE® platform is already established for high-volume deposition and etching in wafer and panel manufacturing. Building on this foundation, we are extending the platform's capabilities to meet the new requirements of advanced packaging. Our roadmap covers three key areas where we are investing and developing future solutions.

Building on a proven base

The Panel Level Packaging (PLP) market is entering a phase of rapid growth and innovation, driven by modular chiplet architectures for AI and high-performance computing. Evatec has been shaping the future of Panel Level Packaging from the very beginning. Almost a decade ago, when this new market segment first emerged, Evatec pioneered panel level PVD solutions right from the start. Today, the company is leveraging its long-standing expertise and strong market presence to drive the next wave of innovation. With a comprehensive roadmap in place, Evatec is continuing to adapt its technologies and product portfolio to the latest developments and future trends, starting from the first projects on 310x310 mm panel formats, then advancing towards even larger panel sizes.

Our activities focus on redistribution layer (RDL) and backside metallization (BSM), through-glass via (TGV) technologies, and reactive ion etching (RIE) for PCB and IC substrate manufacturing.

RDL and BSM roadmap for AI chiplets

Evatec has launched its first dedicated PLP development project for the 310x310 mm format starting from the CLUSTERLINE® 300 platform. This modified system is being engineered to handle and transport panels efficiently, providing higher substrate utilization per cycle compared to 300 mm wafers. Such scaling will allow larger AI chiplets and high-bandwidth memory (HBM) stacks to be processed, boosting throughput and reducing cost per chip.

The development includes new DC/RF sputter and etch modules, a high-performance source and magnet system, and in-situ process control for maximum uniformity and optimized material use. Capabilities under development also target precious metal deposition such as gold with focus on reducing target costs.

The 310x310 mm solution is expected to be available to foundries and OSATs by 2026. In parallel, Evatec is preparing cost-optimized solutions for larger panel formats on the CLUSTERLINE® 600, supporting sizes up to 650x650 mm.

Evatec solution of optimal efficiency

Wafer	Panel	Platform
300 mm		CLUSTERLINE® 300
	300x300 mm	CLUSTERLINE® 310
	310x310 mm	CLUSTERLINE® 310
	510x515 mm	CLUSTERLINE® 600
	600x600 mm	CLUSTERLINE® 600

TGV technology roadmap for large panels

Glass interposers are becoming essential for high-frequency and RF packaging. They require precise drilling, metallization, and dielectric gap filling. Evatec's CLUSTERLINE® 600 platform is being prepared for advanced thin-film deposition on large-area glass substrates.

The roadmap foresees adhesion layer and copper seed layer deposition for TGVs with aspect ratios up to 6:1, with future enhancements aiming beyond 10:1. Ionized plasma capabilities will support conformal adhesion and copper coverage along the sidewalls enabling robust interconnect performance.

In addition to deposition modules, the roadmap includes process integration, automated metrology, and advanced panel-handling concepts (such as enhanced flipper systems) to deliver a complete TGV processing solution for panels up to 600 mm.

RIE and Desmear roadmap for PCB/IC substrates

For organic, polymeric, and glass substrates, Evatec is extending its technology base with plasma etching and desmear solutions. The CLUSTERLINE® 600 and the CLUSTERLINE® 310 with integrated CCP etch modules and atmospheric batch degassing will support advanced substrate pre-treatment.

Planned configurations will enable deep via etching with high aspect ratios and desmear processes optimized for polymer and SiO_2 fillers. Balanced chemistries and Arctic cooling techniques will ensure residue-free via walls, reliable copper adhesion, and repeatable performance across large panels. These developments will provide customers with scalable, production-ready solutions for the evolving demands of advanced PCB and IC substrate manufacturing.

Outlook

With the 310x310 mm project underway and larger-format developments in preparation, Evatec is establishing a roadmap that addresses the full spectrum of future PLP requirements.

Our CLUSTERLINE® platforms will continue to evolve as flexible, high-volume manufacturing solutions, supporting customers as they move from wafer-based packaging to panel formats of increasing size and complexity.