evatec process systems

EDITION 8

LAYERS

ANNIVERSARY EDITION

SEMICONDUCTOR & ADVANCED PACKAGING

New thin film solutions – from next-generation glass core IC substrates to Si & WBG Power

COMPOUND & PHOTONICS

From Quantum Computing to Metalenses, Micro LEDs to Solar Cells – Get the latest news

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Who is Evatec...

We are the **Thin Film Powerhouse**...

...and our **Vision** is to use our deep knowledge in **Thin Film Deposition** and **Material Science** and be the company of choice to enable and drive innovations within the megatrends for **Energy Efficiency**, **Connectivity and Mobility**, **Data Processing** and **Smart Sensing**.

Reflecting on the last 20 years and anticipating the next 20

As we celebrate two decades since the establishment of Evatec in 2004, I take immense pride in our journey so far and the team we have assembled.

Our competencies have grown not only at our Truebbach headquarters, but also across our global organization, positioning us as the reliable long-term partner our customers rightfully expect. Our unwavering commitment to being a "thin film powerhouse" has been the right one and continues to be so, but that does not mean that we do not react to a changing world by continually refining our internal organization, capabilities, and workforce.

Having a profound knowledge of devices, their technology, with market intelligence and employees with skills to identify the needs and expectations of customers two generations ahead is just one example of the goals we set for ourselves. As you explore this year's LAYERS, keep an eye out for the "Who is Evatec" icon – giving a glimpse into some other priorities we set for our company.

New Thin film technology is more essential than ever to deliver mass market consumer devices and applications for the next decades at the right performance and costs – from new panel solutions on CLUSTERLINE® 600 supporting advanced IC substate technology, to new BAW filter solutions for 5G and beyond, enhanced MicroLED technology for Augmented Reality on CLUSTERLINE® 300, and new material development for Heterogeneous Integration, High Performance Logic and Memory.

So here's to our journey over the next 20 years and more, it's one we very much look forward to making together with you, our valued customers.

Andreas Waelti CEO

EVATEC CORPORATE NEWS

CELEBRATING 20 YEARS OF DEVELOPMENT AT EVATEC

Navigating innovation: A conversation with our CTO

We have made internal changes to equip ourselves for the future. Our Chief Technology Officer (CTO), ***Dr. Carlo Tosi***, talks about balancing tradition and change, overcoming technical challenges and how his team approaches innovation.

Can you share some highlights from your background and career journey that led you to the role of CTO at Evatec?

Sure, I'd love to share my journey with you. My academic background is in physics and material science and engineering, which I studied in Italy. I then worked at the Universities of Trent and Florence and at the National Institute for Nuclear Physics before moving to Switzerland. The early part of my career was dedicated to thin films and coatings for tribological applications. I soon moved into the world of semiconductors, focusing on thin film and bulk semiconductor radiation detectors for high energy physics applications. My transition from the academic world to business happened smoothly when I joined Oerlikon Solar in Switzerland. At Oerlikon, I started with the development and transfer of the PECVD production processes from the headquarters' pilot line to the customer's factory, and eventually, I ended up overseeing the integration of all the processes in the production line. This role involved the transfer of production processes globally, which was interesting and challenging! From there, I moved to ALSTOM and joined the Future Technology organization as Group Manager Innovative Components. This was an exciting time as I was part of a team that implemented an open innovation approach to scout new technologies and solutions for future business. This was a particularly insightful experience and taught me a lot about innovation. Subsequently, I joined ABB Semiconductors as a Technology Manager, where I was responsible for the development activities related to bipolar power devices. This role included regular travel between sites in Switzerland and the Czech Republic, with a focus on improving communication and collaboration between the two development teams. Finally, in 2019, I joined Evatec as a Product Marketing Manager, a role that, although business-oriented, required significant technical knowledge. After a period of time as the BU Semiconductor leader, I had the opportunity to become Evatec's CTO, rounding off my career journey wonderfully.

What has shaped your leadership style?

Overall, my leadership style has been shaped by a combination of technical expertise, adaptability, project and product management skills, business orientation and an understanding of the importance of open communication and collaboration. Every little detail can have a big impact when it comes to being successful, and blending creativity with careful execution is essential to successfully complete projects and respond to market needs.

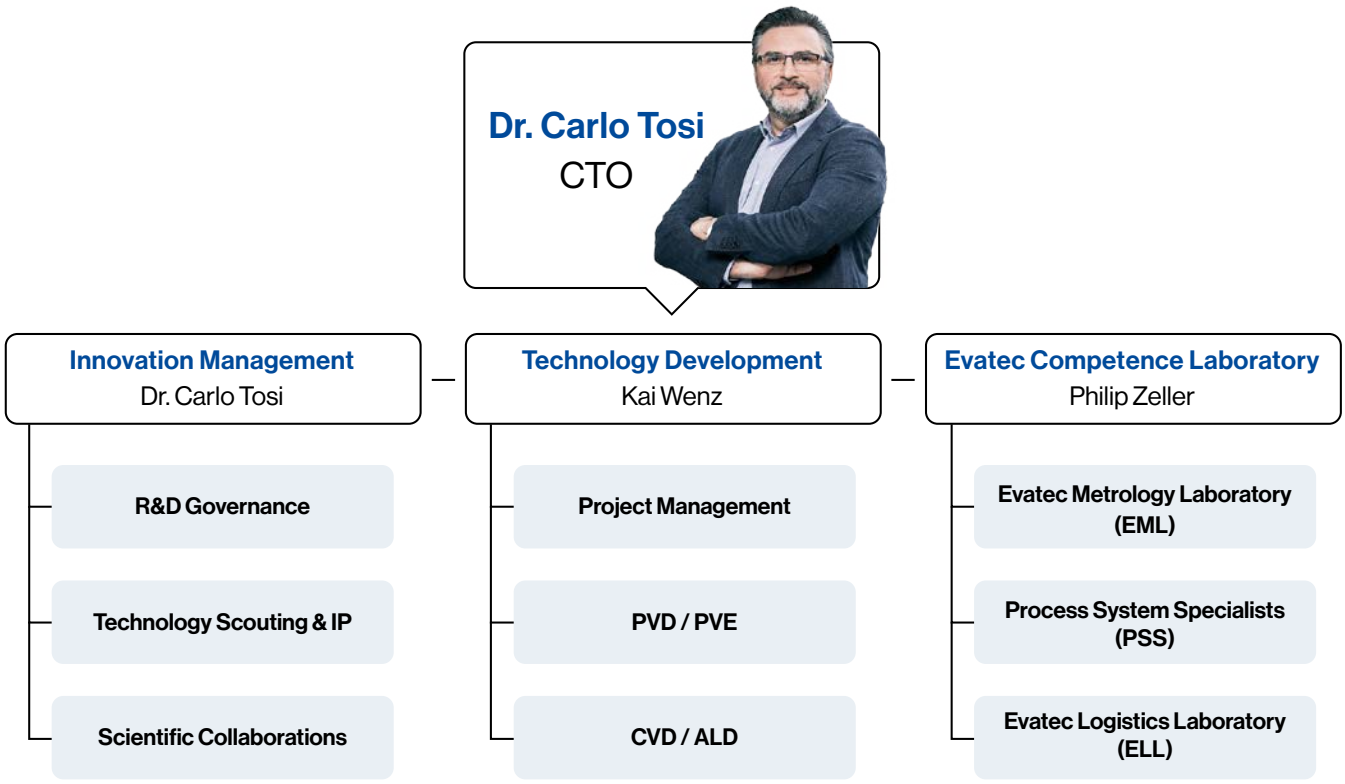
Who is Evatec...

R&D at Evatec

Technology & Market Understanding:
Taking the right decisions in time comes from profound knowledge of devices, their technology, market intelligence and our employee's skills to identify the needs and expectations of customers two generations ahead.

Innovation Strength:
A strong technology portfolio exploits synergies across our markets giving stand out solutions for our customers that put them ahead of the pack.

At Evatec, everyone can come up with an idea, which could become a development project.



CTO Organization at Evatec

What aspects did you inherit from the former CTO, and how have you built upon or transformed them?

He left behind an amazing team, and since taking over I've prioritized fostering an environment where each team member can use their skills and talents to the fullest.

What were the challenges after starting in your new role as CTO, and how did you address them?

The biggest challenge was a major reorganization of our company, including the CTO department. We had to focus on a smooth transition from the old organization to the new one in the initial weeks. We addressed this by defining our innovation process and the procedures necessary for our daily efforts, while at the same time not losing sight of our ongoing development projects. We also worked hard to bring our laboratory operational standard to the highest level. It's a continuous effort and there's much work still to be done. Our goal is to continually innovate not only our products, but also the way we navigate through innovation.

What strategic goals or innovations do you envision for your department?

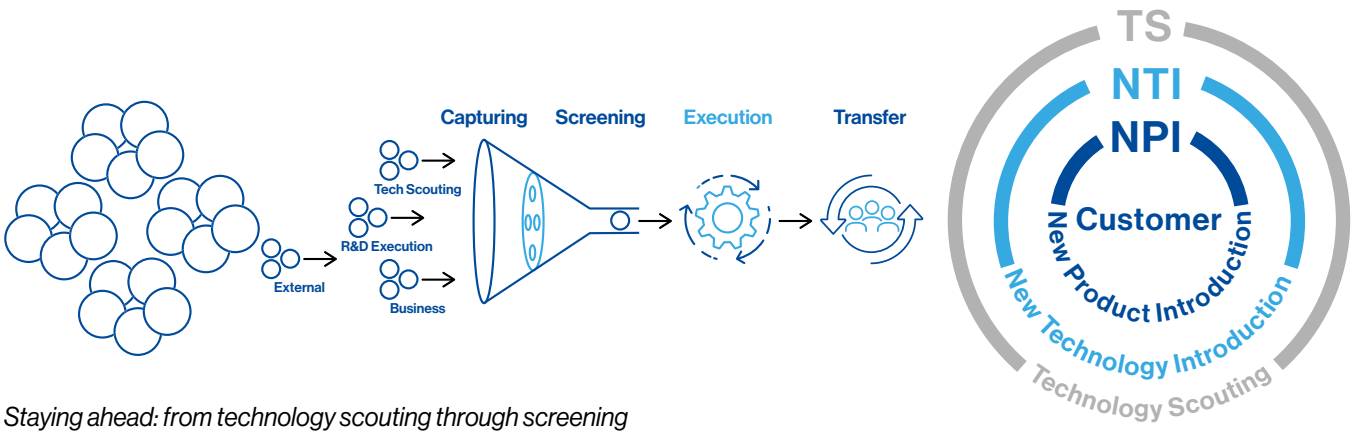
The semiconductor industry is always on the move, breaking barriers and setting new standards at a rapid pace. This evolution is driven primarily by aggressive investments in research and development. Can you imagine that almost 20% of the industry's annual revenue in the US is funneled back into R&D? We are talking about tens of billions of US dollars. As a supplier, we at Evatec know-how critical it is to keep up with this whirlwind of progress. But we don't just want to keep up. We want to lead. And that's why our number one goal is to always be at the cutting edge of our markets.

It's pretty amazing to think about how much digital computing has become a part of our everyday lives. It's all due to the incredible advances in hardware and software. And it's not just that - so many other technologies are also growing at an unbelievable pace. Just think about it - analogue electronics, memory and storage technology, advanced communication solutions, not to mention AI and energy generation and transformation. It's an exciting time to be in this industry.

Evatec already has a strong footprint in the discrete device market. We're talking about Wireless, MEMS, LED, AR, Power and so on. But that's not all. We're continuously growing our product base and refining our process solutions using the latest advanced process control techniques.

However, we're not just focusing on these areas. We're also keen to enhance our solutions for the CMOS frontend of the line, which includes both the front side and the back side of the wafer. For that we are currently working on several development projects, in collaboration with major market players, which will allow us to penetrate the memory business, for example. Packaging and interconnect solutions are also vital. That's why we're paying close attention to emerging trends such as chiplets, 3D integration, and fan-out wafer-level packaging (FOWLP).

Last but not least, we want to do all this following the best innovation and project management standards in order to provide our customers with the quality they expect from a Swiss company. For this, we've created a specialized team to oversee innovation governance, ensuring our customers receive nothing but the best.



Staying ahead: from technology scouting through screening all the way to the best product or technology introduction.

How does your team approach innovation and what processes or frameworks guide idea generation and implementation?

Well, I'll try my best to keep the explanation brief. The R&D Department is composed of three teams, namely "Innovation Management", "Technology Development", and the "Evatec Competence Laboratory". Innovation Management is further structured into three parts: Governance, Technology Scouting & Intellectual Property, and Scientific Collaboration. Basically, Governance is where we define the way Evatec goes through the innovation process. For example, we have structured the Technology Scouting process, the New Technology Introduction (NTI) process and we largely contributed to the redefinition and implementation of the company's New Product Introduction (NPI) process.

At Evatec, everyone can come up with an idea, which could potentially become a development project. All you have to do is present your proposal to the Technology Scouting team. They will assess the proposal's potential and how well it fits with the company's strategy. It's not just technical experts who look at these proposals - business colleagues are also involved. If the proposal passes this screening phase, it might become an NTI project or be framed as an NPI project.

However, only the Product Marketing Manager can submit new product projects (NPI) to the Executive Board. That's because all NPI proposals need to get the buy-in of at least one of our two business fields either Semiconductor & Advanced Packaging, or Compound & Photonics. The idea is to ensure that our innovation efforts are always linked to a return on investment.

Now, we also work with external partners on innovation initiatives. These collaborations are managed by the Scientific Collaborations team. They're in charge of finding new partners and proposing new collaborations.

Moving on, the Technology Development team is where the development projects come to life. The team is staffed with project leaders, engineers, and scientists, and it's they who hold all of Evatec's core PVD/PVE and CVD/ALD technical knowledge.

And of course, we have the Evatec Competence Laboratory (ECL). It's like our playground, equipped with over 30 vacuum deposition systems, representing all of Evatec's platforms, and more than 40 in-house metrology tools, including SEM, AFM, XRD, etc. It's essentially one of the best equipped labs around! We also have a chemical lab to aid our everyday work. We use the ECL for all sorts of things, like hardware, software and process development activities, customer demo and sampling, product maintenance, engineering initiatives, and a whole lot more.

So, that's a nutshell view of our R&D Department. I hope this gives you a general idea of how we're organized!

Give us an example of significant technical challenges your department has overcome?

The team is constantly delivering great results, but I have to give a special shout-out to our PEALD initiative. This was a brand new technology for us and we've managed to develop and launch it successfully. One module is already docked to a CLUSTERLINE® of one of our customers. Right now, we're refining our solution which includes in-situ cleaning. We really think that our PEALD can be a game changer for a variety of applications, especially in a cluster configuration, where you can mix PEALD, PECVD, PVD, and etching all in one system.

What excites you most for the future?

The investment we have made in optimizing our internal innovation processes is starting to pay off and we can focus better on execution of all the projects we have now prioritized, bringing new technologies or processes to market more quickly. There are so many fields where my team sees huge potential. I feel like "a kid in a candy store" so don't be surprised when we bump into each other in the corridor at our headquarters and you see me with a big smile on my face!

You can read more about **PEALD on page 18** in this edition of **LAYERS**

Dynamic Dragons: Powering through Asia with our Prowess

Discover how Evatec developed its organization in Asia and the key role the region plays in the company's growth. From cutting-edge solutions to collaborative partnerships, find out more about Evatec's journey in the dynamic Asian market with ***Kevin Chen***, Head of Evatec Asia.

Can you share the story of how Evatec established its organization in Asia?

Evatec established its first Sales & Service Organization (SSO) in Asia in 2016, starting from South East Asia (Singapore, Malaysia) and expanding to Taiwan, China, and Japan. The SSOs provide direct customer support, enhance understanding of customer needs, and strengthen cooperation and partnership with them directly.

What motivated the company to focus on this region?

Asia's robust market for Semiconductor, Advanced Packaging, Optoelectronics, and Photonics presents significant business opportunities for Evatec. It's our biggest market. The region's mature and cost-effective supply chain, coupled with its advancements in relevant technologies, contributes to Evatec's growth.

What do the people like about working for an international company like ours?

Working for an international company like Evatec offers the opportunity to collaborate with people from around the world in a multi-cultural environment. It also provides exposure to cutting-edge technologies, broadening our perspectives. Swiss quality standards facilitate trust and long-term partnerships with colleagues at our Swiss headquarters.

How has Evatec adapted to the challenges presented by the Asian market?

We need to support different customer types – OSATs (Outsourced Semiconductor Assembly and Test), IDMs (Integrated Device Manufacturer) or Design Houses and their different needs. Of course, there is always strong competition, so we also need to differentiate ourselves. Our Asia Sales & Service Organizations (SSO) have invested heavily in training and transferring know-how to our Asia team members. We are able to provide professional and fast responses to customers. As a company Evatec has also developed relationships on the supply chain side with local Asia experts.

Tell us more about the services of the Asia SSOs?

The main activities of our SSOs are providing sales, marketing and technical support to our local customers. In partnership with our colleagues at Evatec HQ we are continuously looking to develop our Asia business further. Typical day to day activities include a very wide range of tasks, such as promoting Evatec's technologies and products in meetings with customers or in any kind of technical forums or trade shows. We provide services like machine installation, trouble shooting and performance improvement. Collecting customer's feedback as well as market intelligence allows us to support our company in developing the best solution for our local market.

7 SPARE PART
warehouses in 5 countries

>1,100
SYSTEMS
installed

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How has the organization changed over the recent years and what impact has it had on customer satisfaction and business growth?

Back in 2016 when we started out our local know-how was in its infancy, and we had to rely more heavily on support from our Headquarters in Switzerland. However, in 2019 we started to build up the ATTF (Asia Technical Task Force) and an Asia L2 (Level 2) support team in cooperation with our senior management from HQ. We then established an Asia Software Team, TMM (Technical Marketing Management) Team and a Trainer Pool in 2020. Even during the time of the COVID-19 pandemic (2020 – 2022), we continued investing in Asia to strengthen our capability to better serve customers and grow our business. Going forward, we will keep investing in selected Asia sourcing activities to strengthen our support for Asia customers. With all the resources (engineering team, spare parts warehouse, service office etc.) we have invested in Asia, our customers can now get more professional and faster technical support from Evatec than ever.

You now have around 140 team members and 13 offices. How have you managed to foster collaboration and knowledge sharing among team members as the organization grew?

We work with common processes around the world with clear rules and regulations for our new Asia team members to follow. In addition, starting from day one, we introduced and encouraged a "One Asia Team Concept" when we set up the Asia SSOs in 2016. Therefore, our Asia team members who are in different countries share the same work culture and values as a single team. It's all about bringing the right people on board and supporting their integration.

Tell us about the "One Asia Team" Concept and what that means?

The "One Asia Team" spirit is that all employees of our Asia SSOs belong to one big Asia Team. People may still spend the majority of their time working in their home country, but will still need to provide service outside their base location and work together with other colleagues in different countries for specific projects when there is a need. The concept provides lots of benefits for the company as well as our Asia team members such as more flexibility in using our Asia resources to support projects or countries where we need lots of short-term manpower or special expertise. We cooperate closely to manage business using talents we have across the whole team. We share our knowledge and experience with each other so we can grow together. People have a chance to get exposure to various cultures and broaden their view of the world. Employees in our Asia SSOs love the "One Asia Team" Concept and enjoy being part of a big Evatec Asia family!

≈50%
CHF REVENUE
in Asia

13 OFFICES
in major Asian locations – China, Taiwan, Korea, Singapore, Malaysia and Japan

≈140
HEADCOUNT
(> 100 CS) in Jan 2024

What is the role of the Asia Technical Task Force (ATTF) team?

The main tasks for our ATTF include technology transfer from Swiss HQ to Asia, development of local technical solutions, high-skill support (including Asia L2 support, process, software and training), and special project management within the Asia region. Dr. Suresh Singaram leads the ATTF team, which collaborates across Singapore, Malaysia, Taiwan & China.

Give us an example of an innovation the ATTF team has delivered?

In addition to various technical support functions, the ATTF team spent approximately two years developing and optimizing the eLAT software tool. This tool enables rapid analysis of potential technical issues using machine datalogs. We recognize that user-friendly and powerful software is crucial for successful production equipment. We support our specialists within the HQ in developing new software features and capabilities.

The "One Asia Team" spirit – all employees of our SSOs belong to one big Asia Team.

What emerging trends do you see in our markets in Asia and how is Evatec positioned to address them?

I would like to give feedback from two perspectives: **Technology and Production trends:**

1. **Technology trends**: We see that technology developments such as Artificial Intelligence (AI), Augmented Reality / Virtual Reality (AR / VR), 5G / 6G Communication, High Speed / Quantum Computing, Electric Vehicles, happen faster and faster. All require lots of new materials (different wafer or substrate materials), process capabilities (TSV, TGV, WLO, high precision film properties control) and also highly sophisticated machine performance. Evatec invests huge amounts and efforts in R&D activities and in working closely with global key market players / customers (IDM, OSAT, Design House), R&D institutes on developing new technologies which can keep us as a tier one technology solution provider.
2. **Production trends**: The increasing geopolitical tension leading to a Supply Chain Management (SCM) move to the south may mean that more and more market players including device manufacturers, material and equipment suppliers increase their investment and production capacity in southern Asia regions like Malaysia, Singapore, Vietnam, Thailand and India etc. However, as a complete region, Asia will keep its leading role. Our own flexible Evatec organization and our mature team can provide professional support to our customers wherever they are.

Tell us about how Evatec collaborates with local partners and suppliers in various Asian countries.

We are focused on system design and component integration. We collaborate closely with suppliers in Asia, including Singapore, Japan, Taiwan and China. We aim to enhance Asia sourcing and customer support activities to better serve our customers in Asia.

What are Evatec's strategic goals for growing the business in Asia in the future?

Our strategic goals are well-defined and ambitious.

1. **Market Leadership:** We aspire to become the number one player in our served markets. This goal reflects our commitment to excellence and customer satisfaction.
2. **First-Class Customer Support:** Providing top-notch support to customers is a priority. To achieve this, we collaborate closely with our global organization, aligning activities to deliver professional service as a unified team.
3. **Expanding into Emerging Markets:** While traditional markets like China, Taiwan, Korea, Singapore, and Malaysia will remain strong for us, we recognize the potential in emerging regions. We actively participate in the growth opportunities in Vietnam, Thailand and India. These countries are witnessing increased investment and technological activities, making them attractive markets for Evatec's products and solutions. □


OPTIMIZATION
PROCESS

“Ship and Merge” Enhancing flexibility to meet customer demand

Evatec COO ***Patrick Mathys*** tells us about Ship and Merge (SaM), just one of the innovative manufacturing initiatives at Evatec supporting our commitment to efficiency and flexibility to meet the needs of our customers.

So, what is “SaM”?

When global demand for electronic components surges and our customers need to react, SaM can step in to help standardize and accelerate assembly, testing, and shipping of the individual core components within the tools we need to deliver. SaM focuses on lead time and cost reduction, space requirements and resources. With SaM, the individual core modules SPM (Single Process Module), VTM (Vacuum Transfer Module) and E-Racks (switch and generator cabinets) of a standard configuration CLUSTERLINE® 200 platform can already be tested and qualified separately with the help of improved and more sophisticated test procedures with enhanced test benches. These can be standard tests for functionality and quality assurance, but also process tests in the case of SPMs. This means that we can dispense with complete assembly of the system in Truebbach. The merging of the entire system then takes place at the end customer’s site. The complete shipment as a single consignment from Switzerland means that the customer sees no difference to today’s deliveries. Figures 1a and 1b compare a traditional and Ship and Merge approach.

Preparation is key

To ensure the success of our approach, we undertook a comprehensive restructuring of our assembly and testing processes for a CLUSTERLINE® 200 through a series of subprojects.

In the “pull-in” subproject, we streamlined the ordering process by consolidating core modules at a higher bill of material (BOM) level from our subsuppliers. For instance, a VTM is assembled alongside all Treatment Units (TU) and customized components, while an E-rack comes equipped with generators, including connected cables. This approach aims to significantly reduce assembly time at our facility.

Building upon this foundation, the process testing subproject adds another layer of refinement. Here, the core modules undergo rigorous functional and process tests to ensure they meet predefined standards. For example, the VTM undergoes a marathon test with substrates. In the case of the E-rack, the generators are started, and the power is measured, and single process modules (SPM’s) have their gas flow and process parameters recorded. The goal of this thorough testing process is to avoid complete assembly of systems in Truebbach, freeing up space for other customer projects.

Important to note is that the test benches subproject encompasses the development of both hardware and software, as well as the adaption of existing test benches for pull-in and process tests. Notably, a complete new E-rack test bench was developed as part of the initiative and capabilities of our VTM and SPM test benches were massively improved.

Maintaining control of process know-how

Although our subcontractors excel at manufacturing, including implementing the new test approach for modules like the VTM and E-Rack, the assembly and testing of SPM’s, which embody Evatec’s core expertise, remain exclusive to our facility in Truebbach. For logistical efficiency, all individual modules of a system will be sent to Evatec in Truebbach before being consolidated and shipped to our customers as a single consignment.

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Traditional approach including complete system assembly and test prior to shipment

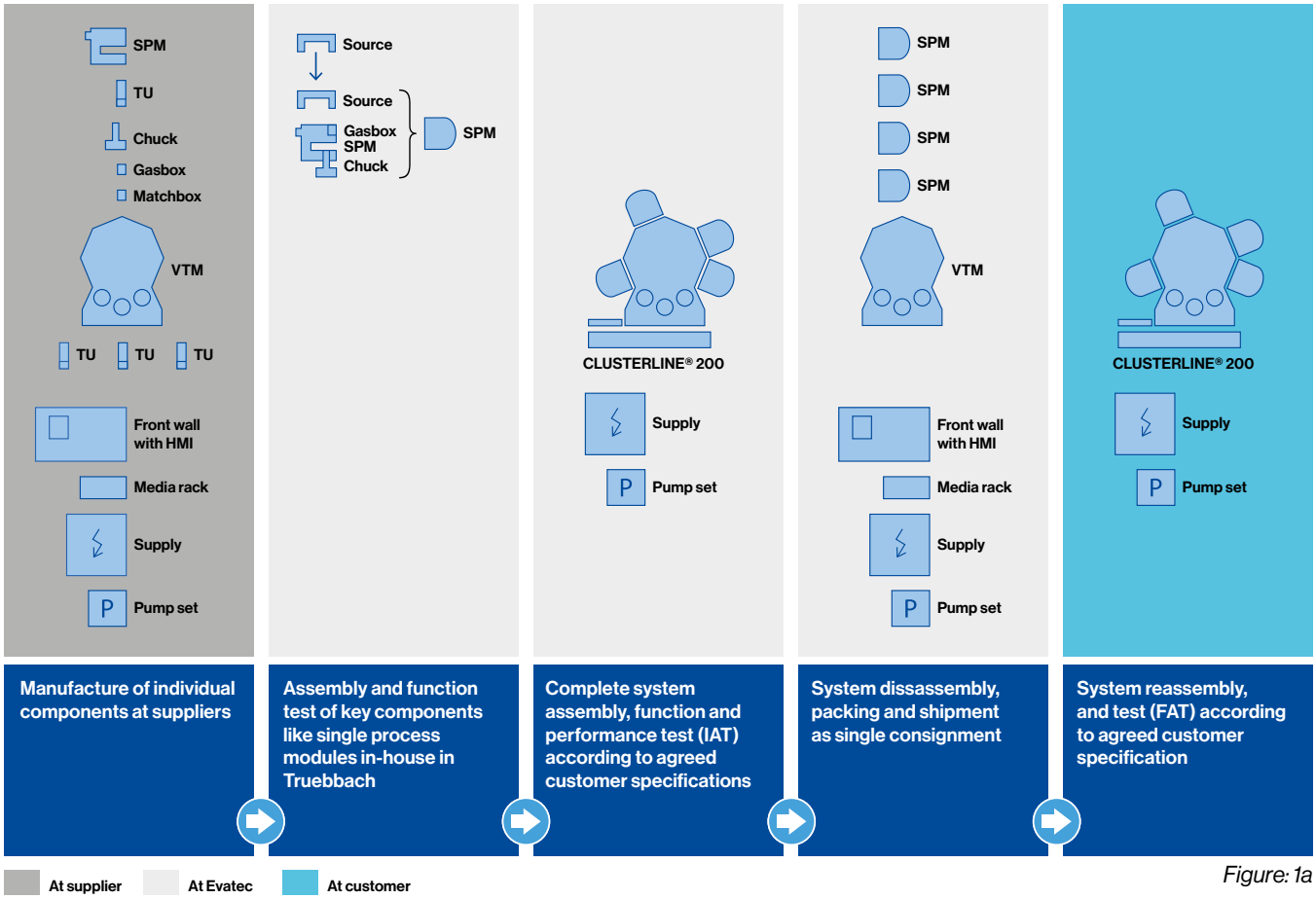


Figure: 1a

Overall benefits for our customers

By implementing SaM, we are not only optimizing our own assembly process but also providing significant benefits to our customers. Here are some advantages:

- **Increased Flexibility**
  SaM enables us to free up capacity in our own assembly line, allowing us to adapt swiftly to changing market conditions. We can react quickly to accommodate the assembly of other tool types beyond those included in the current project. For instance, we can efficiently handle non-standard tools or prototypes tailored to specific customer requirements without compromizing on quality or delivery timelines.

- **Reduction of Lead Times**
  SaM expedites our operations by optimizing assembly and testing processes, resulting in significant reductions in lead times. This effect is even bigger in capacity constraint times, as the SaM line is independent from the normal assembly line.

- **Quality Assurance and Sustainability**

  Consistent Quality: With SaM, we standardize test instructions and protocols, guaranteeing top-notch quality across all repeat builds of standard hardware configurations. This ensures that every product meets our high standards, giving our customers "peace of mind" with each purchase.

  Shared Insights: Our central database offers valuable insights that benefit everyone involved, from our quality assurance team and purchasing department to our service technicians and, most importantly, our customers. By sharing information and working together, we're committed to delivering excellence in every aspect of our products and services. SaM is already showing its worth!

Within the last twelve months we already shipped 17 SaM systems which we could not otherwise have shipped because of the high order backlog in our normal assembly. As the concept is ready and proven we are now able to expand it further to additional processes whenever we see the need.

In essence, SaM isn't just about transforming our assembly process, it's about putting our customers at the center. By streamlining operations, SaM ensures that we can deliver our solutions and tools faster, with higher quality, and with more efficiency than ever before.

Ship & Merge eliminates the need for complete system assembly prior to delivery

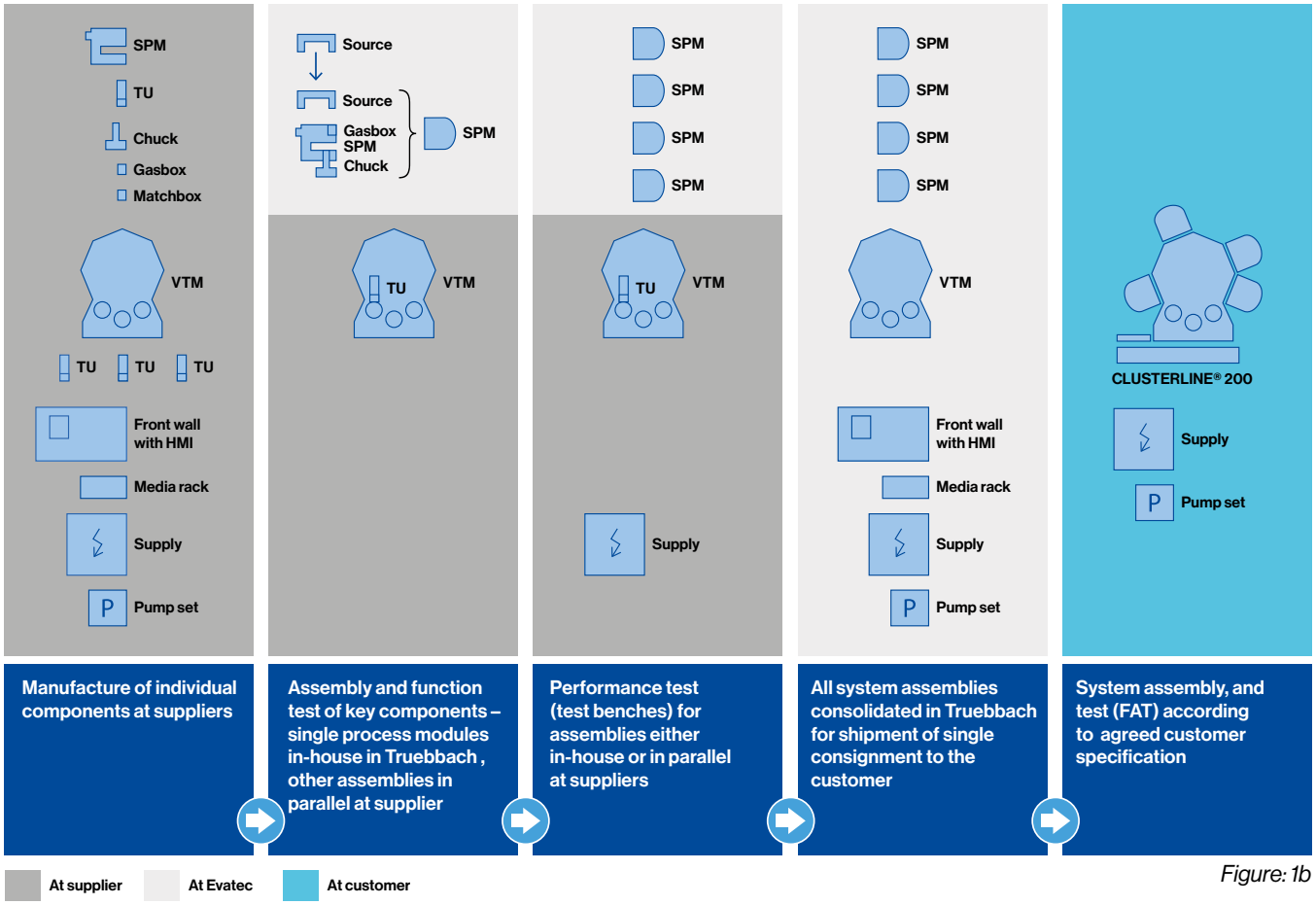
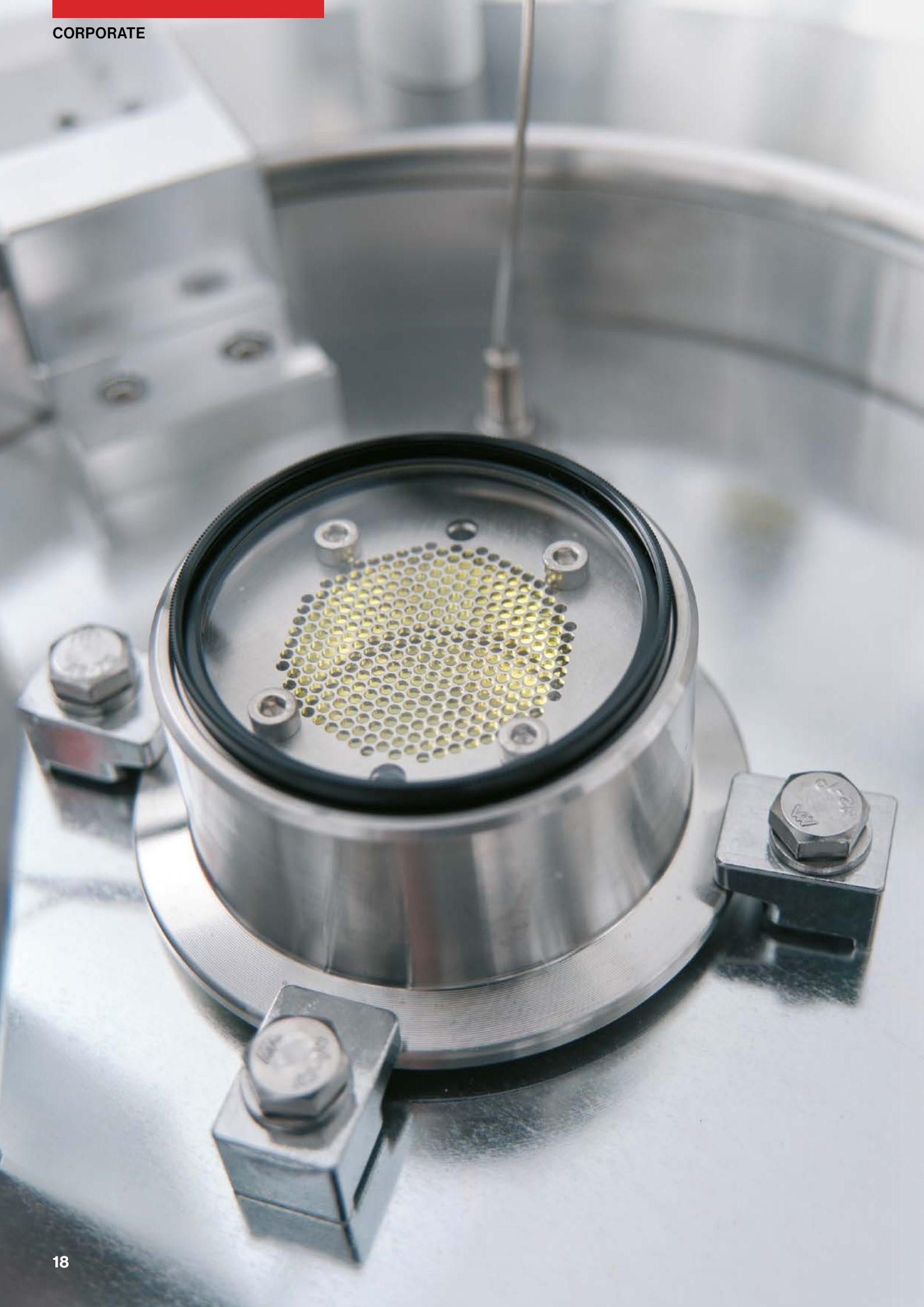


Figure: 1b

It started with CLUSTERLINE® 200, now it continues...

CLUSTERLINE® 200 marked the inception of SaM's journey. Right now, our focus remains on optimizing standard tool configurations and refining our process portfolio for CLUSTERLINE® 200, but as our expertise grows, our goal is to extend the efficiency benefits of SaM to other platforms within our portfolio. While our roots are in Truebbach, where assembly and testing take place, we are committed to innovation that enhances our capabilities and strengthens our partnerships with customers worldwide. We will never produce prototypes with this approach, but we will consolidate and expand, embracing new processes.



PEALD: The new kid on the CLUSTERLINE® block

Dominik Hartmann, Manager Technology Development & ***Dr. Joerg Patscheider***, Principal Scientist, present a new module for Plasma-Enhanced Atomic Layer Deposition (PEALD). As just one of the modules available on the CLUSTERLINE® 200 family, customers can freely combine it in configurations of up to six modules per cluster together with established techniques like sputter, etch and PECVD.

Thin films produced by sputter deposition can be used to address various functionalities such as high optical transparency, defined values of electrical conductivity, specific electromechanical properties such as piezoelectric performance and others. Since sputter deposition is a directional process, it is commonly straight forward to achieve such properties on flat and planar substrates. However, as soon as homogeneous films are required on non-planar surfaces, such as structured wafers and surfaces with radii of curvature much smaller than the wafer dimensions, chemistry-based techniques are well-known for providing solutions to such requirements. Plasma-Enhanced Chemical Vapor Deposition (PECVD) is already well-established in a multitude of applications for films in the thickness range from several hundreds of nanometers up to more than ten micrometers. However, if films thinner than about a hundred nanometers and down to the nanometer range are needed, Atomic Layer Deposition (ALD) and its plasma-supported extension, Plasma-Enhanced Atomic Layer Deposition (PEALD) provides solutions that combine excellent conformality (uniform thickness irrespective of substrate curvature) with atomic precision in thickness.

Evatec's new PEALD module is a novel single-wafer processing station within the CLUSTERLINE® 200 family thats ideal for deposition of thin dielectric films. To reduce deposition temperatures with respect to thermal ALD, a microwave plasma source is used enabling for instance, the preparation of Al_2O_3 films at near room temperature. In contrast to other forms of plasma excitation like RF or even pulsed DC, microwave plasmas have very low sheath voltages. Consequently, the energy of ions impinging from the plasma onto the growing film is only a few eV. This is an important feature if thin film materials sensitive to ion radiation damage need to be deposited. While most materials will not suffer radiation damage at energies below ca. 20 eV, some crucial compounds already show deterioration at lower energies. Examples of ion irradiation-sensitive materials are many group III nitrides such as GaN, InN etc., but also sputter-sensitive oxides, e.g. ITO, MoO_3 and other transition metal oxides, as well as sulfides like MoS_2 and other 2D materials. Only microwave-excited plasmas can provide the favorable conditions required. Figure 1 illustrates a typical PEALD process flow.

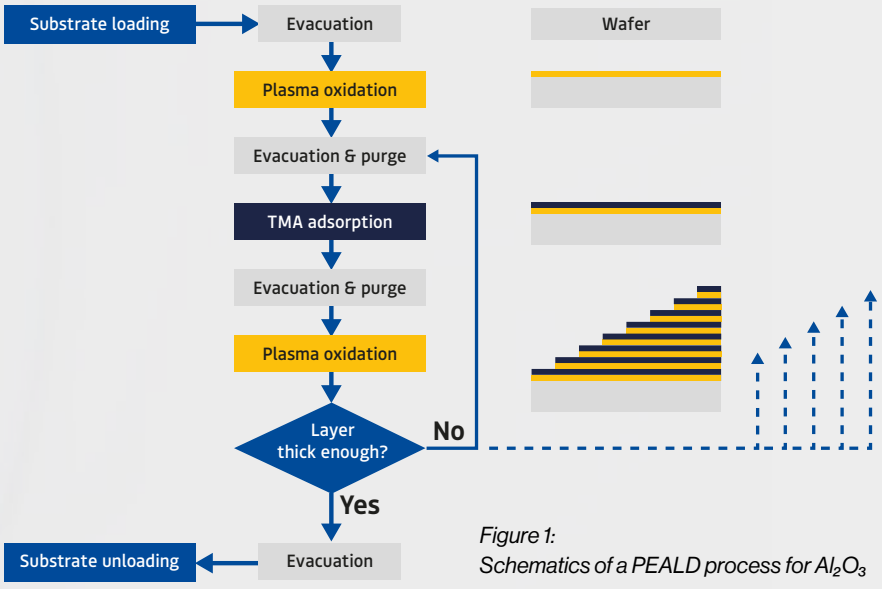


Figure 1:
Schematics of a PEALD process for Al_2O_3

Where ion radiation damage is not of concern for the user, the new PEALD module can be operated with a radio frequency bias on the chuck, allowing full control over the energy of impinging ions in a wide range from a few eV to more than 200 eV. This option allows tuning of various materials parameters of the grown films such as density, refractive index and microstructure.

The use of an arrangement of high-strength permanent magnets outside the process chamber enables this new module to reach Electron Cyclotron Resonance (ECR) conditions. This leads to very high plasma densities which allow almost complete reactions during the plasma step (i.e. during oxidation and nitridation processes) at low temperatures.

In addition to the substrate biasing possibility, the PEALD module is equipped with a heatable substrate holder for temperatures of up to 500°C. While this is 200°C too high for almost all PEALD processes, post-deposition annealing *in-situ* is possible with this device. This opens up new ways to tailor selected properties of the previously prepared films without compromising the PEALD deposition process.

The system is set up to use two different metal precursors, which enables deposition of ternary films such as $SrTiO_3$, Ta-C-N etc. with varying elemental ratios. Ternary oxides, e.g., ITO as well as multilayer structures of the type ABX (X being a non-metal) can also be prepared. The design of the module and processes have been rigorously optimized to achieve minimal precursor consumption and reduced cost of ownership. A special carrier configuration allows for two-side deposition of substrates in a single run, while maintaining the same layer thickness on both sides.

To counteract potential issues with particles formation due to deposits on the reactor's inner walls, the module can perform different cleaning processes like plasma-enhanced chemical *in-situ* cleaning procedures.

To illustrate the perfromance of the module, alumina films with thickness up to 100 nm were prepared at 200°C. Figure 2 illustrates the attained homogeneity of refractive index (@633 nm) of a 45 nm thin layer.

The mean refractive index value is 1.65 at 633 nm with a uniformity of better than ±0.5%, with a layer thickness uniformity of <1%. These layers show carbon contents below 1 atomic percent.

Being a member of the single process module family of the CLUSTERLINE 200®, the new PEALD module can be combined with other modules, e.g. metal layers by sputtering to realize any desired combination of layers on one cluster tool without breaking vacuum. Tools configured in that way can be used to achieve layer stacks of various thin film materials, e.g. piezo-active systems with an oxide capping layer.

Get in touch!

Are such combinations of various techniques on one single platform missing in your tool portfolio?

Does this versatile module fit into your existing CLUSTERLINE® 200 units, or are you considering a cluster just with PEALD modules? We will be happy to discuss the various options with you!

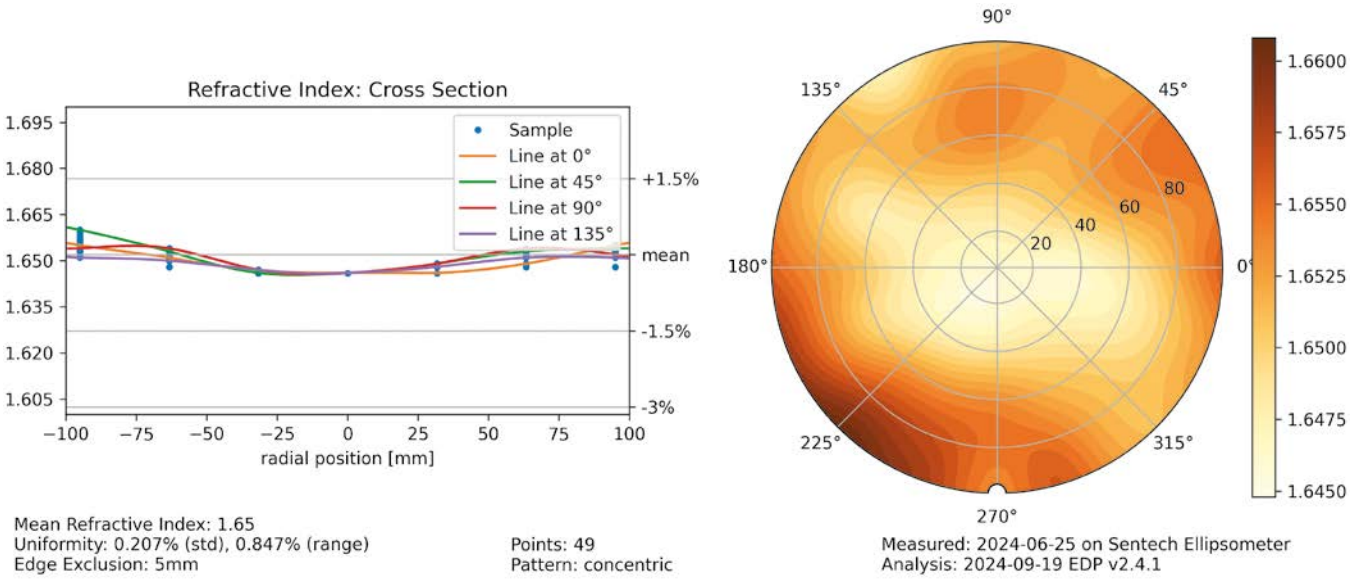


Figure 2: Refractive index uniformity of a 45 nm thin layer of Al_2O_3 prepared by PEALD

Why Evatec PEALD?

Excellent conformality:
Homogeneous film thickness, even on complex geometries.

Precise thickness control:
Ideal for very thin films.

Consistent film properties:
Ensuring optimal material quality.

Flexibility:
Integration of PEALD module alongside PVD, PECVD & etch on CLUSTERLINE® 200.

Process characteristics and module features

Process temperature:
RT – 500°

Deposition pressure:
$2 \cdot 10^{-3}$ – 0.2 mbar

Plasma excitation:
ECR @ 2.45 GHz

Gas lines:
Up to 9

Precursor vessels:
2 or more

Want to know more?

Not familiar with the CLUSTERLINE® platform? Then why not watch the short CLUSTERLINE® family video to learn about Evatec's range of solutions on 200, 300 and 600mm.

To learn more about PEALD contact your local Evatec office

"We've carefully designed a comprehensive equipment relocation service to minimize disruption and ensure a smooth transition"

Moving made easy: Seamless machine relocation for your Evatec equipment

At Evatec, we understand that moving your valuable thin film equipment can be a daunting undertaking. Downtime disrupts production schedules and can significantly impact your bottom line. That's why we've carefully designed a comprehensive equipment relocation service to minimize disruption and ensure a smooth transition. ***David Dietsch***, Product Marketing Manager Customer Service, takes you through everything you need to know about our service, complete with a real-life example to illustrate the process.

Planning is paramount

The key to a successful machine move is careful planning. Our team of experienced and certified field engineers will work closely with you to create a customized relocation plan. Every detail is considered, from the initial pre-inspection to the final handover. This collaborative approach ensures a seamless and efficient process, minimizing downtime and maximizing productivity.

Benefits of utilizing Evatec's relocation expertise

When you choose Evatec for your machine relocation needs, you gain access to several compelling benefits:

- **Detailed planning and preparation:** We work hand in hand with you to develop a comprehensive plan that covers all aspects of the relocation. From pre-dismantling checks to re-commissioning at the new site, we leave no stone unturned.
- **Tailored options:** Recognizing that every relocation is unique, we offer three levels of service: **Light**, **Standard**, and **Full**. Choose the one that best suits your specific needs and budget.
- **Unwavering support:** Our team remains by your side throughout the entire process. Should any unforeseen issues arise, we address them promptly, ensuring a seamless relocation experience.
- **Experienced professionals:** Our relocation specialists have extensive experience in handling your equipment. You can rest assured that your valuable equipment is in capable hands.

OPTIONS	LIGHT	STANDARD	FULL
Planning / preparation tool relocation	✓	✓	✓
Pre-checks on and off site	✓	✓	✓
Health check	✗	✓	✓
Baseline data collection	✓	✓	✓
Decommission of equipment	✓	✓	✓
Organization of transport	✗	✗	✓
Re-installation	✓	✓	✓
Start up	✓	✓	✓
Functional test and handover	✗	✓	✓

Your role in the relocation process

While Evatec manages the relocation itself, your cooperation is crucial for a successful transition. Here's how you can contribute:

- **Review of consumables:** Work closely with our team to assess the remaining life of consumable parts within the equipment. This assessment will help determine if replacements are needed before or after the move.
- **Site support:** Leverage your team's expertise during the isolation, connection, and testing phases at both the original and new locations.
- **Transport equipment:** The necessary transport equipment will have been provided during the initial system installation. However, you are ultimately responsible for transporting the equipment to the new location.

Considerations for obsolete parts during a relocation

Relocating equipment that is 7 years old or more can be a concern, especially if you suspect it contains obsolete parts. Evatec understands these challenges and offers guidance to ensure a smooth transition for your legacy equipment. Here's what we recommend when dealing with potentially obsolete parts during a move:

Consumables: Planning for replacement
Consumables, such as gaskets and O-rings, are essential to maintaining proper sealing and functionality within your equipment. Over time, these parts can degrade and lose their effectiveness. When relocating older equipment, it's important to consider the age and condition of consumables. Evatec recommends proactive replacement planning.

Consumables, especially those that are not replaced for long periods of time, can lose their elasticity and sealing properties. This can lead to leaks, contamination, and potential damage to equipment during transport or recommissioning. Ensuring that replacements are available in advance avoids delays and ensures a smooth restart at the new site.

Consideration of obsolete parts: A holistic approach
We recommend looking at the relocation process as an opportunity to take a holistic approach to obsolete parts. Here's why:

- **Uncertain functionality:** There's a chance that obsolete components, especially after the stress of transportation, may fail to function when restarted. Proactive replacement during the move minimizes downtime and ensures optimum performance at the new location.
- **Retrofit efficiency:** Replacing obsolete parts during the relocation offers significant efficiency benefits. With the equipment already decommissioned and readily accessible, retrofit installation becomes a more streamlined process compared to retrofitting at a later date.

Evatec support: Retrofits before re-installation

To maximize efficiency and minimize downtime, Evatec recommends that all necessary retrofits are in place before the move begins. Our team can assist you in identifying the appropriate replacement equipment and ensure that it is installed at the new site during the re-installation phase. This proactive approach streamlines the relocation process and ensures that even your legacy equipment will also perform optimally in the new location.

By following these recommendations and utilizing Evatec's expertise, you can relocate your older equipment with confidence, even if it contains obsolete parts. We'll work with you to ensure a smooth transition, minimize downtime, and breathe new life into your valuable machines.

Our relocation service in action: A customer story

Picture this: A cutting-edge sputter tool nestled in its original facility, humming with precision and purpose. But change is afoot – the customer has decided to relocate it to a brand new, state-of-the-art production line. The stakes are high; even a small hiccup in the process could disrupt their carefully orchestrated production schedule. So, they opt for our Standard Relocation Package and take care of the transport themselves.

Planning the move

Our team goes into action, working closely with the customer's engineers. Here's what happens:

- **Site check:** We meticulously examine the entire transport route, from loading ramp to destination. Together with the customer, we ensure that there are no spatial constraints along the transport route. We also check that the new site meets the equipment's facility requirements.
- **Health check:** Think of it as a thorough medical examination for the sputtering tool. We assess critical components, run backups, perform visual checks and identify any maintenance required. After all, a healthy tool is a reliable tool.
- **Baseline data collection:** We collect baseline data - a reference point for assessing the performance of the tool after installation. This data becomes our compass along the way.

The relocation process

Once the planning phase is complete, the relocation dance begins:

- **Decommissioning:** Carefully and deliberately, we say goodbye to the sputtering tool in its original home. Utilities are disconnected, process cooling water is drained, and cables are marked for quick identification during installation. Each component is secured for the journey ahead.
- **Transportation:** The customer steps in and provides the initial transport equipment. They orchestrate the tool's safe journey to its new home - the gleaming production line awaiting its arrival.
- **Re-installation:** Our engineers perform a ballet of precision. The sputtering system pirouettes into the new facility, perfectly aligned with the utility connections. Daily progress updates flow like choreography notes to ensure everyone stays in sync.

Start-up and handover

As the curtain rises on the final act:

- **Start-up:** The tool awakens, following established procedures. Systems initialize, gas lines purge, and functional checks dance across the stage. It's showtime!
- **Functional testing:** Extensive tests unfold to ensure the sputtering tool is operating within optimal parameters. The audience - our customers - hold their breath in anticipation of a flawless performance.
- **Baseline data comparison:** Our service engineers revisit the health check points. Is the system as vibrant as before? The answer is in the data.
- **Handover:** The grand finale! With all systems verified, we formally present the tool to the customer's production team. Detailed documentation accompanies the handover, like a backstage pass to operational changes. The customer steps into the spotlight, ready to qualify the sputter tool's role in their production once again.

Considering relocation?

Are you considering relocating your valuable thin film equipment? Don't let the process become a roadblock.

Evatec's relocation services can:

- ☑ Ensure a smooth transition
- ☑ Minimize downtime
- ☑ Maximize your productivity

Contact your local Evatec Sales and Service organization today and let us start planning your move.

Spare Parts | Support | Training | Retrofits

Evatec's services

Watch our video to learn more about our portfolio of services that will help you get the most out of your Evatec tool.

ECL – Supporting customers with small scale production & thin film characterization services

Head of Evatec Competence Laboratory ***Philip Zeller*** gives us an update on the latest capabilities in the ECL and how we are now expanding the services available to customers helping them not only with technology development and prototyping, but also small scale production and quality control in their daily business.

ECL – Ready to support customers in deposition and characterization

Evatec's ECL was established back in 2019 as a center for collaboration with technology partners and customers. It brought equipment and people together in an environment optimized for the best sample production, networking, information exchange and creative thinking. For the last 5 years, it has been a place where customers from around the world joined Evatec process engineers working together on the development and optimization of their next generation thin film processes.

And now it's time to make capabilities of ECL available to customers needing to characterize films deposited within their own facility where they don't have the metrology tools, or needing small scale production support, e.g. as an interim solution whilst they are busy ramping up their own production facilities.

ECL – A lab like a fab

The ECL is an easy place to work- housing both deposition tools and measurement equipment within a central measurement laboratory (EML).

At the heart of the ECL lies a portfolio of thin film tools with advanced control capabilities in a range of configurations to support applications across advanced packaging, power, wireless, MEMS, optoelectronics and photonics. System architectures are available to handle substrate sizes up to 650mm x 650mm.

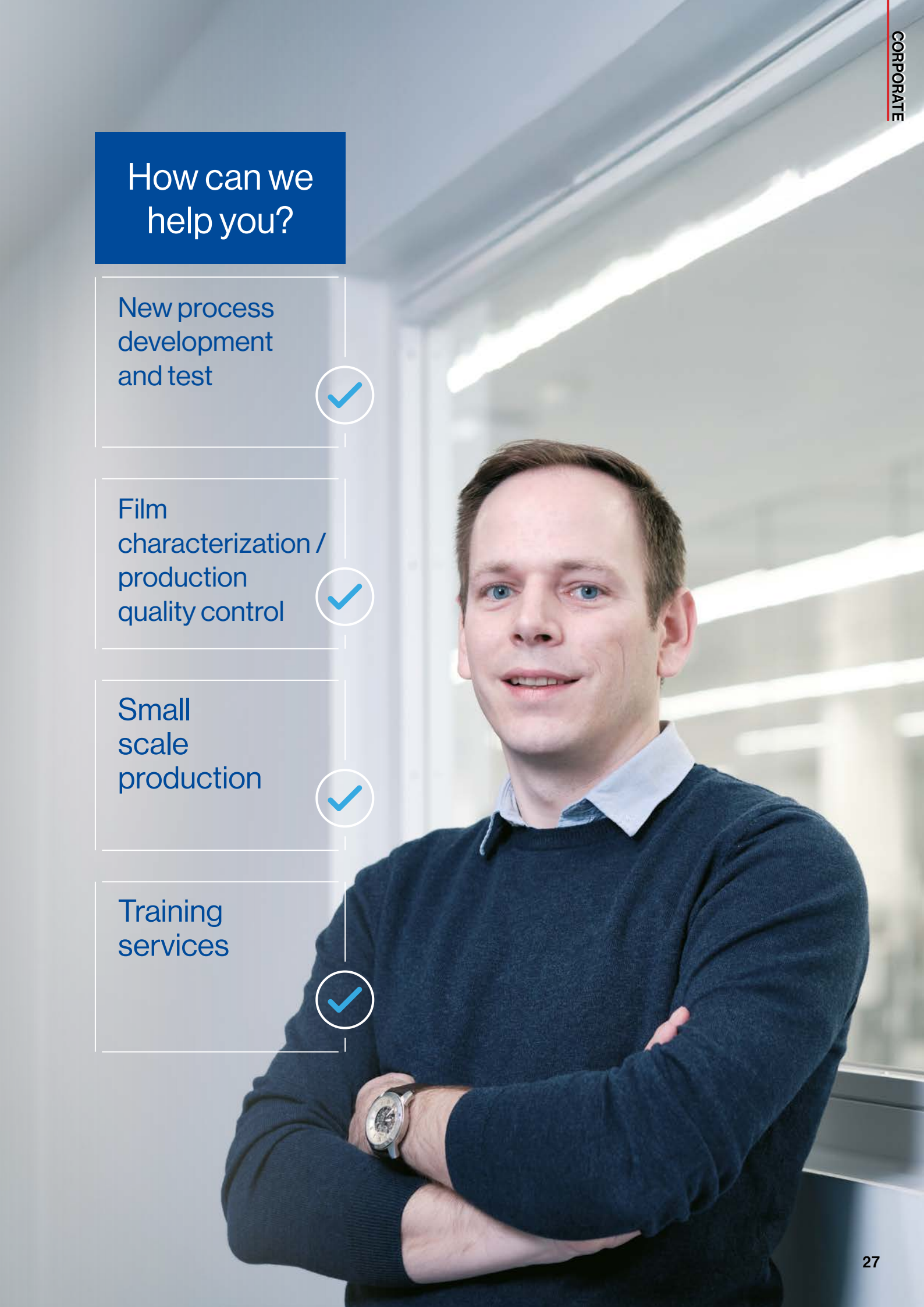
Table 1 summarizes the range of tool architecture and typical processes available within the fab.

Tool architecture types	Process technologies	Substrate handling / loading	Processes	APC capabilities
▪ Batch ▪ Cluster ▪ Inline	▪ Etch ▪ PECVD ▪ PEALD ▪ Sputter ▪ Evaporation	▪ Manual ▪ Cassette-to-cassette ▪ AFEM ▪ Single wafer processing ▪ Batch processing	▪ Dielectrics ▪ TCOs ▪ Metals ▪ Piezoelectrics ▪ Soft magnetics	▪ Plasma Emission Monitoring (PEM) ▪ Broadband Optical Monitoring (GSM)

Table 1: Summary of ECL capabilities

How can we help you?

- New process development and test
- Film characterization / production quality control
- Small scale production
- Training services



Thin film characterization and quality control

The EML is a hub for metrology experts.

Equipped witht tools ranging from basic mechanical profilometers to advanced instruments like AFM, SEM, XRD and XRF, the EML has constantly enhanced its capabilities for advanced characterization of the deposited thin films.

The AFM provides detailed surface topography information with sub-nanometer resolution.

XRD offers insights into crystalline grains within a film, enabling the determination of crystal structure, lattice distance, grain width, crystal quality, and orientation. Additionally, we can measure instrument pole figures and reciprocal space maps for more sophisticated film structure analysis.

X-Ray Reflectometry allows us to measure film thicknesses (typically from a few up to 150nm) and roughness, including multilayer systems and their buried interface roughness.

XRF enables precise, non-destructive film thickness measurements in the sub-nanometer range and provides information about the elemental composition of a sample.

The latest addition to the metrology lab is the Zeiss FIB-SEM. This tool allows us to capture images with information on the topography and the composition of a sample. In combination with its Focused-Ion-Beam (FIB) it allows us to capture images of structures such as trenches and vias and analyze the conformity of the deposited films. Figure 1 illustrates a typical case study.

The EML and its measurement tools are all conveniently located at the heart of the ECL.

The full range of metrology techniques available to customers is illustrated in Table 2.

The ECL – A perfect production environment

Needless to say, the ECL is the perfect production environment of 3000 square meters with a range of clean room spaces down to ISO 4 and particle levels are measured online to maintain a consistent environment. Highly experienced Evatec staff operating the deposition equipment and making thin film characterization measurements on behalf of customers have access to the expertise of Evatec's application and process engineers.

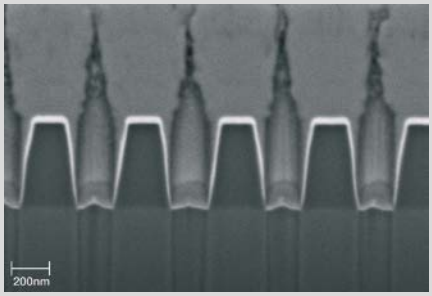


Figure 1: Case Study – Analysis of 3D structures

We observe silicon blind vias covered by a tantalum layer, which appears as the brightest element in the picture. This tantalum layer was deposited using our advanced long-throw sputtering configuration.

Although the FIB/SEM technique does not match the resolution of TEM, its significantly faster processing speed makes it invaluable. Possessing this metrology tool in-house enables us to perform exceedingly efficient and rapid optimizations of sidewall and bottom coverage, a critical advantage as feature sizes diminish and IC designs evolve into three-dimensional structures.

Method	System	Characterization of	Sample size
Atomic Force Microscopy (AFM)	Park Systems NX20	Topography, surface roughness	Up to 200mm
X-Ray Diffraction & Reflectivity (XRD & XRR)	Bruker D8 discover	Crystallinity & crystall orientation, thickness (5 - 150 nm), density	Up to 300mm
X-Ray Fluorescence Spectroscopy (XRF)	Rigaku XRF	Composition, thickness (sub nm - mm)	Up to 300mm
Scanning Electron Microscopy (SEM) / Focused Ion Beam (FIB)	Zeiss Crossbeam 550 L (Gemini II)	Topography, cross section / resolution: 2 nm / magnification 12x- 2E6x	Up to 300mm
Electron Dispersive X-Ray Spectroscopy (EDX)	BRUKER QUANTAX EDS (Xflash 410)	Composition	Up to 300mm
Ellipsometry	Woollam SE M-2000F / Sentech 500Adv, SE 800-PV & SENResearch 4.0	Optical properties (n,k), thickness (1 nm - 10 µm) / (wavelength range: 245-2500 nm)	Up to 300mm
4 point probe	4Dimensions Polytec 333A DI V5.5R1 / 4Dimension 280 TCI & 280 BM 1003 / KLA-Tencor OmniMap RS100	Sheet resistance (0.001 - 8E11 Ω/Sq)	Up to 300mm
Spectrophotometry	Perkin Elmer Lambda 950, 750, Spectrum II / Essentoptics GmbH Photon RT	Transmission, reflection (wavelength range: 175 - 3300 nm & 1200 - 28500 nm)	50 x 50mm
Reflectometry	ProMicron NanoCalc 300 / Mikropack Metrology Systems NanoCalc 2000	Film thickness (10 nm - 20 µm) / wavelength range: 210 – 2500 nm	Up to 300mm
Laser level & Interferometry	Frontier Semiconductor FSM 128L / KLA-Tencor Flexus FLX 2320 / Toho Technology FLX 3300-T	Wafer bow, radius, stress (1 - 4 gpa) / dual-laser	Up to 300mm
Optical Microscopy	ProMicron Leica INM 200	Particles (sensitivity: 1 µm)	Up to 200mm
Laser Light Scattering	UnitySC Lightspeed / NanoPhotonics Reflex 300 TT 150	Particles (sensitivity: 50 nm) / haze	Up to 300mm
Contact Stylus Profilometry	Veeco Dektak V 300 Si & V 150 / KLA-Tencor Alpha Step 500 & 600, P 16	Thickness (1 nm - 1200 µm) / stress	Up to 300mm
Profilometry	Eichhorn & Hausmann MX 204-8-21 V	Wafer thickness, bow, warp, TTV (Total Thickness Variation)	Up to 200mm
Magnetometry	Shb Instruments MESA 200 (in-plane) / Kerr magnetometer (self-made)	Magnetic properties	Up to 200mm
Contact Angle	Krüss FM40MK2 Easy Drop	Surface tension	Up to 100x100mm
Life timer	Sinton WCT120 & Suns-Voc 150	Life time of charge carriers in Si	Up to 200mm

Table 2: A wide ranging list of Thin Film characterization techniques

Want to know more?

To learn more about the new services available and to get a quote please email: **philip.zeller@evatecnet.com**

Our market organization is ready to serve you!

As of January 2024, Evatec embarked on an exciting new chapter. With the launch of our market- and product-focused organization, we have united customer-centric strategies and market orientation with cutting-edge equipment and process development under one roof. This new structure strengthens our ability to deliver tailored, innovative solutions and exceptional support across the fields of Compound and Photonics, as well as Semiconductor and Advanced Packaging. ***Ralph Zoberbier***, ***Admir Asanoski*** and ***Jakob Bollhalder*** introduce our business fields and their activities.

Jakob Bollhalder
Head of Compound & Photonics

We are more than happy to introduce Evatec's new organizational structure, which unites our strengths from previous business units with product development, customer engineering, and process innovation. This strategic integration allows us to better support your journey within two dedicated sectors of the electronics industry.

In the Compound and Photonics business field, we are focused on pioneering solutions for Optoelectronics, including LEDs and laser diodes, MEMS, and Wireless technologies like BAW and SAW filters. In addition our work is particularly driven by the latest developments in augmented and virtual reality layers, as well as the growing demand for photonic integrated circuits.

In Semiconductor and Advanced Packaging, we offer cutting-edge technologies for front- and backside layers of Power Devices, advanced packaging solutions, and heterogeneous integration applications. As the industry advances, we are committed to also delivering the innovative technologies needed to overcome challenges in frontend integration and panel processing, which are crucial to meeting the performance demands of Artificial Intelligence (AI).

You can read more about our developments and acheivements in the next two chapters of this edition of LAYERS.

>>>>

Ralph Zoberbier
CMO

Admir Asanoski
Head of Semiconductor
& Advanced Packaging

Compound & Photonics – Leveraging know-how across market segments to keep the lead!

Just like within semiconductor and advanced packaging, huge changes in technology are and will continue to enable the mass market introduction of exciting new consumer devices. **Jakob Bollhalder**, Head of Compound & Photonics, introduces the primary market segments and the technological innovations propelling growth.

Key Market Segments and Drivers

- Within **Wireless Communication**, enhanced capabilities using 5G are already a feature of the smart devices in our hands and the drive is already on to deliver even faster speeds, lower latency, and greater connectivity – 6G here we come!
  - ☑ From high performance SiO_2/SiN insulating layers to AlScN piezoelectrics for filtering and metal electrodes Evatec is supporting advanced SAW (Surface Acoustic Wave), BAW (Bulk Acoustic Wave), and RF Power technologies.

- Technologies within **Optoelectronics** like Micro LED Displays will see significant growth through mass market applications, initially in wearable technology, then expanding into augmented reality (AR) and automotive displays.
  - ☑ From low-damage TCOs that reduce fabrication damage and improve device longevity, to metal contacts ensuring reliable electrical connections, and mirrors that enhance light manipulation and efficiency, Evatec's solutions are trusted by the world's leading manufacturers. Additionally, our anti-reflective coatings significantly improve output.

- **Photonics** is a sector with huge opportunities for the future and the integration of photonic components on a single chip. Photonic Integrated Circuits (PIC) is just one approach that will revolutionize performance and costs for many new consumer applications.
  - ☑ Successful market introduction calls for thin film production solutions in areas like input couplers, e.g. BTO or for integrated light connections (e.g. SiN) and Evatec is your partner!

- **MEMS** (Micro-Electro-Mechanical Systems) technology offers significant growth potential in areas like Magnetic Sensing: (new advances in actuation technologies) and Quantum Computing (advanced materials and precise fabrication techniques)
  - ☑ In the realm of quantum computing in particular we offer know-how for superconducting films such as Nb, aTa, Al, and Ti. Pilot lines established with market leaders means Evatec is well placed to support the industry as it takes off at the end of the decade.

Who is Evatec...

Why choose Evatec as your partner?

Listening to and innovating together with our customers is at the heart of our philosophy. Just like market needs develop so must our production solutions. That means providing platforms inherently flexible by design which can be adapted as necessary to the changing needs of individual customers, be it higher throughputs, more demanding layer specifications and sometimes both! Working together with our customers and suppliers in long term partnership is a "win-win" for us all.

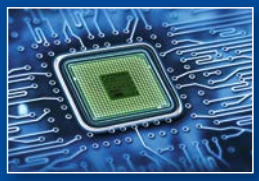
Our aim is simple – to deliver the best customer value in the industry.

Semiconductor & Advanced Packaging – A great place to be!

In the ever-evolving landscape of electronics, the Semiconductor & Advanced Packaging sector is a hugely exciting area of innovation and growth. **Admir Asanoski**, Head of Evatec's business in this sector guides us through some of Evatec's activities covering three market segments, each with its own technological advances and market drivers.

Key Market Segments and Drivers

- **Power Devices** such as transistors, diodes, and thyristors are essential for a myriad of electronic systems. The demand for these devices is surging, driven by the electrification of transportation, the integration of renewable energy, and stringent energy efficiency regulations. These components are integral to the functionality of electric vehicles, solar and wind power systems, and energy-efficient consumer electronics.
  - ☑ Evatec leads the way with a diverse range of metallization processes for power devices made from Si, SiC, or GaN. Our portfolio includes solutions for frontside and backside contacts, protection layers, and other applications, all tailored to meet the specific needs of our customers.



- Within the **Frontend Market** our focus is on advanced node devices, such as Logic ICs and Memory products, driven by the ongoing trend towards miniaturization and integration. The demand for advanced CMOS ICs is fueled by the need for smaller, more powerful, and energy-efficient devices, as well as the requirements of AI and big data analytics.
  - ☑ Evatec offers interconnect metallization processes and niche applications such as warpage compensation used within the process flow of a 3D-Nand Memory, ensuring the highest quality and reliability in end products.

- **Advanced Packaging techniques** are revolutionizing the performance of semiconductor devices by integrating multiple components into a single package. Employing technologies like 2.5D and 3D integration, WLP, and PLP brings greater miniaturization and enhances electrical and thermal performance.
  - ☑ As market leader, Evatec delivers sputter solutions for advanced packaging processes with a unique system concept for wafer-level packaging delivering industry-leading R_c performance and outstanding CoO. With more than 10 systems installed around the globe our solutions for panel-level packaging, including Fan-Out processes and TGV, are at the forefront of IC panel advances.

Our Mission

We provide innovative thin film production solutions and services in our selected markets. Our process solutions ensure top performance, cost efficiency and uncompromised quality. We honor our committments and deliver on time.

Teamwork
Collaborate to achieve success

Innovation
Drive and foster innovative solutions

Responsibility
Take ownership of our actions

Committment
Consistently deliver on our promises

Integrity
Uphold the highest ethical standards

Delivering the best customer value in the industry

SEMICONDUCTOR & ADVANCED PACKAGING NEWS


20
ANNIVERSARY
CELEBRATING
20 YEARS OF
DEVELOPMENT
AT EVATEC

Reducing the environmental impact in the PCB / IC-Substrate industry

AT&S experts ***Gernot Schulz*** and ***Christof Wernbacher*** togther with Evatec's ***Roland Rettenmeier*** explain how the CO_2 footprint of PCB manufacturing can be reduced by reducing raw materials and wet processes, optimizing product build ups and introducing dry processes.

AT&S – Playing its part

The Electronics industry as well as the PCB industry are undergoing a massive change in manufacturing. Governments, OEMs and customers all require a reduction of the CO_2 footprint and a resource-efficient use of raw materials, support materials, energy and water throughout the entire value/supply chain. The "Green Deal" is the European Union's response to this major global challenge for the future. Manufacturing companies are among the key players in the environmentally friendly economic development of tomorrow and are called upon to contribute to solving these challenges with their ideas and innovations. Various measures are available for this purpose: Switching to renewable energy, climate-friendly mobility, resource-conserving value chains, material innovations and intelligent product developments that are designed entirely for recycling.

Product Carbon Footprint – Wet chemical processes are the main contributor

The production process of printed circuit boards generally consisting of mainly wet chemical processes such as etching, galvanic or cleaning. Figure 1 gives an overview on how different production processes from classic PCB production contribute to the overall Product Carbon Footprint of PCB (PCF). Therefore, a sample product consisting of a 10-layer PCB with PTH and Laser Drills manufactured in AT&S production facility in HTB was chosen for this study. Several Energy and Chemical consumptions along the production chain were measured and broken down on product level. The contribution of the different process steps is highly dependent on PCB design such as number of layer, complexity and advanced technologies used. In general a significant amount of emissions are related to the energy and chemical intensive galvanic and etching process steps. Both are standard processes within the PCB production landscape and form the basis of a subtractive manufacturing approach. Since sustainability is in addition to costs and technology becoming a further focus point, additive manufacturing approaches which do not rely on wet chemical processes are becoming of greater interest.

One important part and door opener into additive manufacturing is the sputtering / PVD process. On one hand it improves PCB manufacturing from a technology point of view, on the other hand it allows us to reduce the amount of subtractive production processes.

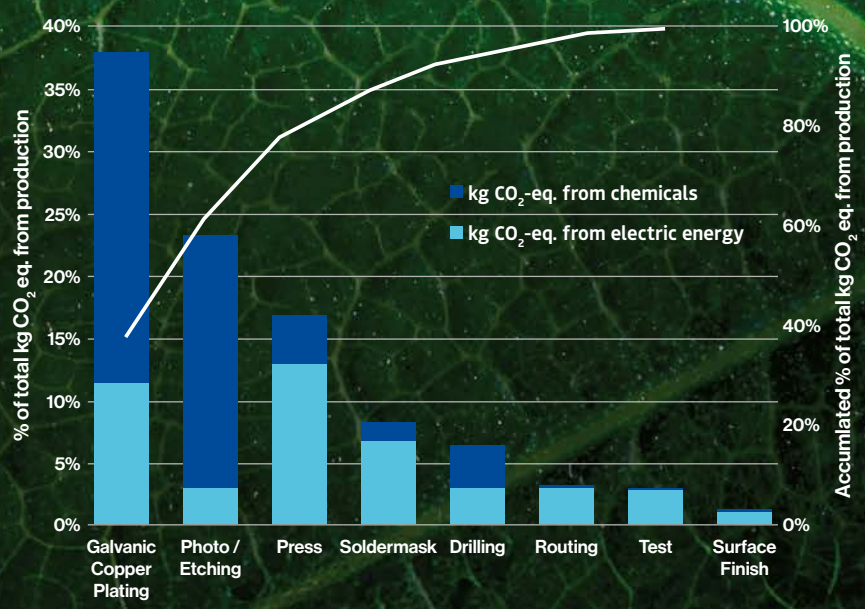


Figure 1: Carbon Footprint of different production processes

Novel technologies as a key to more sustainable products

To further substantiate this correlation, a study was initiated which allowed direct comparison of the environmental footprint between a PCB produced with Sputtering/PVD processes on Evatec's CLUSTERLINE® 600 versus a PCB produced with standard technology. This study was done as part of AT&S' initiative to better understand the environmental impact of different technology platforms and process groups. Therefore, the boundaries of the study were set around processes dedicated to a specific technology. The focus of the study was so called embedding technology, which allows the embedding of ICs as well as active and passive components directly into the PCB which gives numerous advantages especially from a technological point of view. Different technology levels are available with Center Core Embedding (CCE) being the current standard technology. The more sophisticated technology which is currently under development uses a Sputtering/PVD process.

For the comparison the main process steps of both technologies were quantified regarding their consumption of energy, chemicals, process gas and water. The environmental impact of the different input streams was assessed with a combination of primary data from material and energy supplier as well as data from ecoinvent database.

Figure 2 shows the comparison of the Carbon footprint between both technologies. The new generation embedding technology shows a significant reduction, mainly due to a reduction of energy and chemical consumption. This reduction can be achieved because of the more efficient product design becoming feasible with new technology. The process gas which is only used in the new generation embedding technology does not have a serious impact on the overall result.

As an additional benefit, which is not considered in the assessment, the new generation embedding technology also increases the utilization of the panel according to the die to package ratio, which basically indicates how densly the Integrated Circuits (IC) can be placed onto the Package. Considering this improvement, the advantage of the new technology is even more significant.

In addition to embedding technology, Sputtering/PVD processing has the potential to increase the opportunities in PCB design not only in terms of technological aspects, but also in terms of more sustainable design. Different Life Cycle Assessments of PCBs have shown that reducing layer counts as well as reducing the size of a single PCB for better utilization of the production panel leads in most cases to a significant improvement of the Product Carbon footprint.

Improvement beyond carbon footprint

The focus of the industry and branch in Europe is definitely on reduction of the carbon footprint due to the several large initiatives such as the EU Green Deal or the Paris Agreement which are focusing on Greenhouse gas reduction. But to gain a holistic picture of environmental impact it is also necessary to take a look on further influences (for example environmental impact categories according to CML-2016). For all these categories beyond the carbon footprint AT&S plans to extend these assessments to create a more complete picture. But especially for PVD/Sputtering process and the opportunities coming with this technology an even larger improvement is expected than for the carbon footprint, since the reduction of wet chemical processes and therefore chemistry usage is highly connected to other benefits e.g. reduction human toxic substances, acidification potential or nutrification potential. Due to the fact that Sputtering/PVD is also considered as one key technology for miniaturization of electronic components such as PCB or IC Substrates, it can also make its contribution to reducing the global e-waste problem. With miniaturization approaches the relative amount of e-waste can be reduced by simply reducing the volume and mass of the electronic components. Overall more dry process steps in PCB production will lead to less impact on the environment from the industry sector.

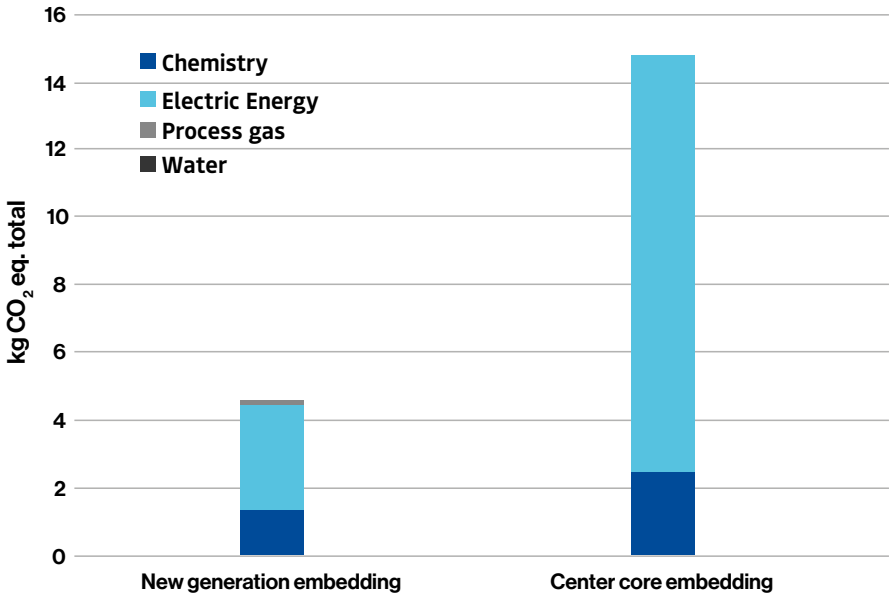
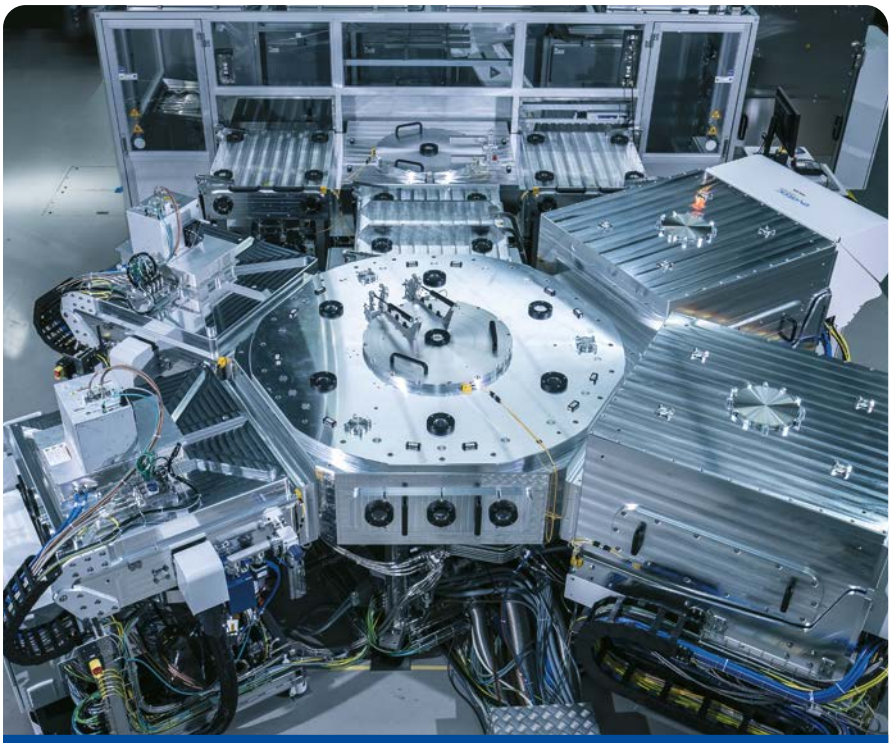


Figure 2: Carbon Footprint of new generation embedding technology compared to standard embedding technology

Heading in the right direction

The PCB industry has been trying to find novel technologies and processes to reduce the amount of wet chemical subtractive processes within the manufacturing landscape since many years. The internal and external pressure to reduce the environmental footprint of PCB production is now bringing an additional argument to go in this direction. Sputtering/PVD process technology now seems to be the most promising approach. Direct comparison with conventional technology shows a significant improvement from both sides – ecologically and technologically. Currently the technology is used for special use high end cases, but when it finds its way to more commodity use cases also high volume applications can profit from the environmental impact reducing processes.



CLUSTERLINE® 600

To read about Evatec's CLUSTERLINE® 600 sputter platform and some of the most recent technological developments go to page 40 or visit **evatecnet.com/products/clusterline-family/clusterline-600**

A view of AT&S*

Technology and digitalization are having an ever-growing impact on our lives and are increasingly shaping our daily routines at home and at work. The advances achieved in these fields in recent years are truly breathtaking and have created crucial momentum for growth in every sector of the economy. As a global technology enterprise, AT&S is actively involved in these developments and plays a decisive role in shaping the digital world of tomorrow. This also represents an enormous responsibility, which AT&S has always accepted and fulfilled through its forward-looking vision, pioneering investments in research and development, and responsible use of resources. The high-end PCBs and IC substrates AT&S supplies influence future industry standards, products and applications in a number of key industries.

Want to know more? Visit **https://ats.net/en/** or complete the contact form at **https://ats.net/en/contact/**

**Source: AT&S website*

CLUSTERLINE® 600 Perfect for next generation IC-substrates too!

The potential benefits of moving from wafer to panel processing including much higher material and process utilization are already well documented (Figure 1). Evatec's Senior Product Marketing Manager ***Roland Rettenmeier*** takes us through some of the recent developments on the well established CLUSTERLINE® 600 platform. These updates in capability make it the perfect choice for customers when setting up manufacturing capability for emerging markets like advanced IC-substrates for applications such as Artificial Intelligence, and other High Performance Computing applications.

innovation
onto

Evatec Collaborates with Onto Innovation in Panel Level Packaging Applications Center of Excellence

To find out more about the co-operation read the article

Advanced Packaging Technologies for the future – Building on a common portfolio of process technologies

Evatec's CLUSTERLINE® 300, CLUSTERLINE® 600 and HEXAGON, feature the same process concept for Advanced Packaging:

- Atmospheric batch degas for preparing substrates with organic load for best in class vacuum processing
- ICP or CCP Etch technology (with arctic cooling) for highly uniform etch prior to deposition
- Long life PVD sources for lowest cost of ownership in high volume manufacturing

CLUSTERLINE® 600 – A proven pedigree in high volume manufacturing

Evatec's CLUSTERLINE® 600 panel processing tool was built leveraging the know-how gained across Evatec's wafer level processing platforms over many years and has already established itself as the market leading system for panel processing. Built around a central Vacuum Transfer Module (VTM), the tool can be equipped with up to 5 single process modules (SPM) for etch or deposition. An atmospheric front end module (AFEM) handles substrates in and out of FOUPS stationed on up to 6 Load Ports (LP). Pre-processing via Evatec's unique Atmospheric Batch Degasser (ABD) followed by two stage pumping brings substrates into vacuum in perfect condition for any etch and deposition processes. A typical configuration is shown in Figure 2.

By the start of 2024 there were more than 10 CLUSTERLINE® 600 working in volume manufacturing around the world. The latest developments on the tool make it ready to handle next generation IC-substrates.

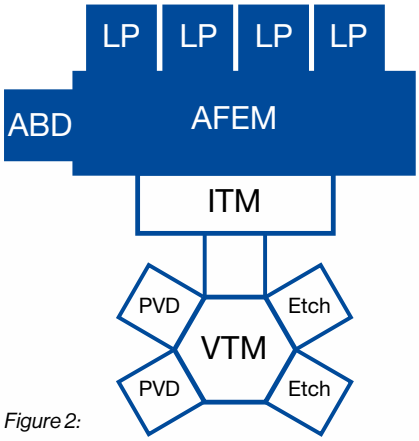


Figure 2:

Panel Level Packaging – Bringing much higher material and process utilization

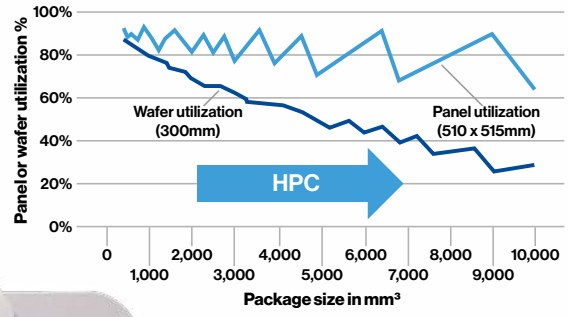
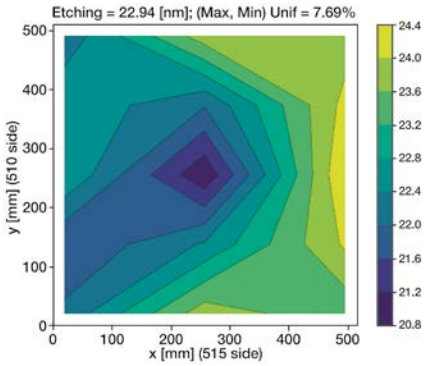


Figure 1:

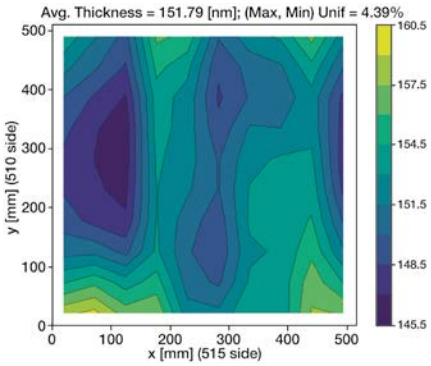
Some typical process results

Low contact resistance (R_c), excellent adhesion and low particles are paramount. Typical process performance results of etch and deposition processes for Ti and Cu are shown below.



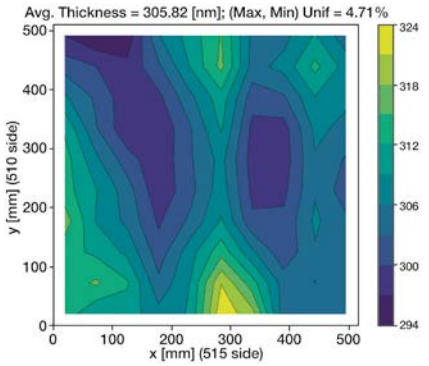
Etch

Etching uniformity better than 10%, for etching amount of 20nm (SiO_2 equivalent), with etch rate higher than 0.15nm/s.



Ti deposition

Thickness uniformity better than 6% for 150nm Ti deposition. Sputter rate higher than 100nm/min and Rs ≤ 75 uOhms*cm.



Cu deposition

Thickness uniformity better than 6% for 300nm Cu deposition. Sputter rate higher than 200nm/min and Rs ≤ 3.5 uOhms*cm.

New tool features now available

Ready for advanced substrates

Newly designed end effectors for handling thin substrates down to 100µm thickness and recessed chucks with full "Keep Out Zone" (KOZ) functionality ensure that active areas are not touched during handling and processing.

High performance robust handling – flipping

The latest AFEM design can accomodate up to 6 Load Ports and features a substrate flipper for double sided processing.

A view from Yole Group

The Glass era starts in the advanced IC substrate and semiconductor equipment industries.

The advanced packaging industry is at a new inflection point with the arrival of glass as a new core material. Announced by Intel in September 2023, this next generation of Advanced IC substrates will be adopted to overcome the limitations of organic core substrates and easily meet the demands of high-performance computing (HPC) and AI trends, opening new options such as flexible form factors and better mechanical stability.

Glass, as a material, offers superior dimensional stability, thermal conductivity, and electrical properties compared to the built-up organic substrates. However, glass introduces challenges in handling and processing, requiring precise care during manufacturing. Additionally, inspection and metrology processes for glass substrates necessitate specialized equipment to ensure quality and reliability.

Despite these challenges, the adoption of glass core substrates is driven by the demand for larger substrates and the technological trend toward chiplets and heterogeneous integration.

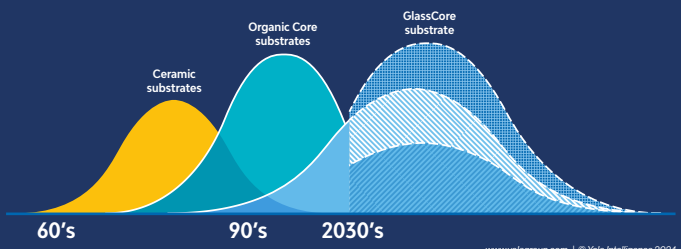
Within this landscape, Through Glass Via (TGV) technology is crucial, facilitating higher connection density and superior signal integrity for high-speed circuits. While TGVs offer performance benefits, they also present manufacturing challenges and higher production costs. Recent advancements in TGV-related patents are aiding the commercialization of glass core substrates.

The synergy between glass core substrates, organic core substrates, and panel-level packaging (PLP) is driving the adoption of panel-adapted equipment by offering enhanced chip density, reducing costs, and improving manufacturing efficiency and yield. As GCS technology matures, it promises to redefine the advanced packaging landscape, particularly for AI accelerators and servers, paving the way for next-generation chip designs and packages.

The increasing growth of AI and its next-generation AI accelerators is driving a significant increase in chip package sizes. Current AI accelerators typically have package sizes around 70 to 80 mm. However, the growing need for larger packages, exceeding the limits of organic substrates at 120 by 120 mm, presents a challenge to the advanced packaging industry. To address this demand and offer a cost-effective solution, the industry is shifting towards panel utilization and related equipment, enabling the production of larger chip packages at reduced costs.

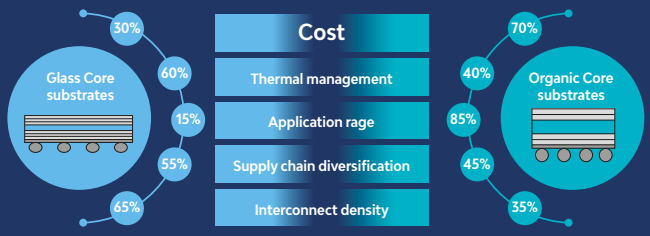
Market adoption trends of Glass Core Substrates

Source: Satus of the Advanced IC Substrate Industry report, Yole Intelligence , 2023



Advanced IC Substrate – comparison with Organic Substrate material

Source: Satus of the Advanced IC Substrate Industry report, Yole Intelligence , 2023



YOLE Group

About the author

Bilal Hachemi, Ph.D., is a Technology & Market Analyst, Semiconductor Packaging at Yole Group.

Working within the Manufacturing & Global Supply Chain activities at Yole Group, Bilal contributes daily to the analysis of packaging technologies, their related materials, and manufacturing processes.

Previously, Bilal carried out experimental research in the field of nanoelectronics and nanotechnologies, focusing on emerging dielectric materials and their ferroelectric applications. He (co-) authored several papers in high-impact scientific journals and participated in several international conferences.

Bilal obtained a Ph.D. in nanoelectronics in 2022 from the Grenoble Alpes University (France), and he studied at IAE Grenoble for a management master's degree.

Study of Cross-Contamination in Multi-Chamber PVD Systems Used for High-Throughput Seed Layer Deposition

Modern WLP application require PVD systems that can deliver low and stable contact resistance (R_c) at high throughput. HEXAGON is an excellent candidate to fulfill this role. This study demonstrates that chamber-to-chamber cross-talk during continuous run is negligible compared to the residual outgassing of the etched wafer itself as explained by ***Kay Viehweger*** from Fraunhofer IZM-ASSID, Germany, and Evatec's Senior Process Engineer, ***Dr. Patrick Carazzetti***.

Abstract

Higher interconnect density in WLP applications increases the importance of interconnect quality, measured by contact resistance (R_c). UBM and RDL metallization are key steps. HEXAGON shows 50% lower Rc and 40% higher throughput than the CLUSTERLINE®. Cross-contamination mainly comes from residual outgassing of etched PBO wafers.

Introduction

Wafer-level packaging (WLP) technologies play a key role in supporting the continuous miniaturization, increased functionality and better power efficiency required by the ever more sophisticated system-on-chip (SoC) and system-in-package (SiP) architectures [1,2]. The downscaling of the critical design dimension and the concomitant increase of I/O density per unit area, has increased the need for a tighter control of the contact resistance (R_c). R_c is referred as the ohmic resistance between the uppermost level of the active circuitry and the metal routing to the bumps. In fact, R_c is directly related to the performance of the packaged device, such as the overall power consumption and signal integrity [3-5]. High-volume manufacturing (HVM) relies on magnetron sputtering for the deposition of adhesion/seed layers that are necessary for the subsequent formation of under bump metallization (UBM) and redistribution layers (RDL). The sputtered PVD stack primarily provides the adhesion function to the underlying pad and organic dielectric passivation, and also a conductive layer for electroplating. Prior to the sputter deposition, state-of-the-art multi-chamber PVD systems perform dedicated pre-treatment steps to improve the metal adhesion to the dielectric. First, the degas step drives out moisture from the dielectric film, which is especially necessary for hydrophilic organic materials, such as Polyimide (PI) or Polybenzoxazole (PBO) [6-8]. This is to avoid that excessive water molecules re-emerge during the subsequent fabrication steps. Secondly, the wafer is sputter cleaned using a mild Argon plasma bombardment to remove oxides from the metal contacts (usually Al or Cu pads) formed through the organic passivation. This etch clean, is typically an inductively-coupled plasma (ICP) process operating at low bias voltage (<600 volts) to avoid device damage. Next, without breaking vacuum, the wafer undergoes the sequential deposition of the Ti-adhesion and Cu-seed layers. The load of organic volatile byproducts generated during the non-selective Ar sputter etching must be efficiently removed from the system to avoid contamination of the other process stations. Since the final device performance is measured only upon completion of the entire WLP process, it is critically important to manage the contamination level and to ensure that especially the Ti-adhesion layer capping the I/O contacts, is deposited in a clean environment that prevents oxide re-growth and contamination from hydrocarbon species.

Previous research presented a benchmark of throughput and R_c performance of two competing PVD systems architectures used in the manufacturing of UBM and RDL metallization. These PVD systems are the HEXAGON and the CLUSTERLINE®, respectively. Data generated in wafer-level chip-scale packaging (WLCSP) have demonstrated that the HEXAGON can consistently deliver 50% lower R_c baseline for a corresponding 40% higher throughput [9]. Further hardware developments of the HEXAGON platform were done to boost its handling speed. This improvement has demonstrated that the HEXAGON can maintain low and constant R_c values even at record throughput of 80.0 wafers/hour [10]. Beside the overall better performance obtained on the HEXAGON compared to the CLUSTERLINE®, there is an aspect of the former platform that has not been sufficiently investigated. In fact, the indexing concept itself, based on the simultaneous transfer of all wafers, would make this platform critically exposed to cross-talk between the different process stations. This can result in an excessive contamination of the PVD chambers, primarily due to the load of organic volatiles species propagating from the ICP sputter etch chambers. The consequence could be the contamination of the metal interfaces, which may adversely impact the R_c of the fabricated device.

This work presents a side-by-side comparison of the cross-contamination dynamics occurring in the HEXAGON and CLUSTERLINE® PVD systems employed in their current HVM

configuration. Residual Gas Analysis (RGA) is used to characterize the level of contamination in two strategically important locations of both platforms. These are the vacuum transport module (VTM) and the Ti deposition chamber.

Hardware Characteristics and Process Strategies

The main hardware characteristics, process strategies and performance of the two platforms are compared in Table I. More than a decade ago, the "arctic" ICP etch chamber was introduced to tackle new process challenges arising from the poorly vacuum compatible organic passivation materials, which were starting to see widespread use as dielectric layers in WLCSP applications [9]. The concept basically consisted in actively cooling the process environment by means of an external chiller unit supplying coolant fluid to the pedestal and the chamber shields.

Essential Hardware Characteristics, Process Strategies and Performance of the PVD Platforms Presented

The chilled pedestal coupled with Argon back-gas provides in-situ cooling to the substrate during process. Whereas the active cooling of the metal shields counterbalances the heating effect induced by the plasma process, thereby mitigating additional outgassing from the organic material residues already present in the chamber. In addition to the active cooling, the pumping efficiency of the chamber was also improved. Furthermore, aluminium pasting was introduced as a periodic conditioning procedure to keep R_c low and stable and to extend the shields lifetime [11]. The Atmospheric Batch Degas (ABD) was developed to deal with heavily outgassing substrates, such as the Epoxy-mold compound (EMC) used in Fan-Out wafer-level packaging (FOWLP) applications [9]. In the ABD, a batch of wafers is loaded into a heated metal cassette and exposed to a laminar flow of N2 for a minimum time of 20 minutes.

Several advantages inherent to its configuration, as well as the dedicated process strategies allow the HEXAGON platform to reach best-in-class R_c at higher throughput compared to the CLUSTERLINE®. Two aspects which are believed to play a key role are discussed hereafter. First, the faster chamber-to-chamber transfer time allows to minimize the time interval between the end of the ICP sputter etch and the beginning of the sputter deposition of the Ti-adhesion layer. This is believed to decrease the risks of recontamination or reoxidation of the cleaned contacts. Secondly, the strategy of splitting the ICP etch amount in two chambers is beneficial to contain the residual outgassing load in the first chamber, while the contact cleaning is completed in the second chamber relatively free from volatile contaminants.

Typically, a multi-chamber PVD system operates in a regime where the throughput limitation comes from the longest sequence executed in one of the process chambers. Steady-state operation mode is achieved when consecutive batch of wafers are processed in the system without interruptions. The residence time in the ABD does not represent the bottleneck as long as neither its capacity, nor the process time impact the regular flow of wafers to sustain continuous loading of the airlock. The handling speed of the platform comes into play during the chamber-to-chamber wafer transfer. From the R_c standpoint, it is therefore strategically important to setup the process flow in such a way to minimize the transfer time occurring between the end of the ICP sputter etch and the beginning of the Ti deposition. Practically, this is achieved by imposing the etch sequence to become the time bottleneck of the entire flow. In the case of the HEXAGON, where the etch amount is split over two chambers, the process sequence is programmed in such a way that the second chamber becomes the bottleneck.

Topic	Platform type	
	HEXAGON	CLUSTERLINE®
Transport in atmosphere	▪ Combined Gantry / SCARA 5-axis robot	▪ Combined Gantry / SCARA 5-axis robot
Transport in vacuum	▪ Central servo motor with revolving carousel	▪ Bisymmetric arm robot
Wafer transfer time in vacuum [sec]	▪ 13.0 (older generation) ▪ 8.0 (new generation)	▪ 28.0 – 30.0
Airlock cycle time [sec]	▪ 25.0-28.0 (single unit) ▪ Wafer capacity: 1	▪ 50.0-56-0 (2 units operating in parallel) ▪ Wafer capacity: 2
Pumping system (high vacuum)	▪ Airlock: turbo ▪ Process chambers: turbo ▪ VTM: turbo and cold traps	▪ Airlock: turbo ▪ ICP etch chamber: turbo ▪ PVD chambers: Cryo ▪ VTM: Cryo
Degas strategy	▪ Atmospheric Batch Degas (ABD) for WLCSP & FOWLP	▪ Single-wafer vacuum degas for WLCSP ▪ ABD for FOWLP
Cooling station	▪ Dedicated process chamber with chilled pedestal, wafer clamp and back-gas	▪ Not implemented
ICP sputter etch strategy ("arctic" chamber)	▪ Two serial etch chambers (50/50 split etch amount) ▪ Chilled pedestals and metal shields (-30°C)	▪ Single etch chamber ▪ Chilled pedestal and metal shields (-30°C)
Aluminium pasting strategy (ICP chamber)	▪ Automated by SW, with aluminum plates stored in atmospheric buffer station	▪ Automated by SW, with aluminum plates stored in atm. or vacuum buffer stations
Throughput [wafers/hour]	▪ 90-100 (handling limited) ▪ 45-55 (process limited[a])	▪ 40-45 (handling limited) ▪ 26-34 (process limiteda)
Rc [mΩ] (source OSATs)	▪ 7.0 ± 0.3 ▪ Al pasting frequency every 10 prod. wafers	▪ 7.5 - 12.0 ▪ increased Al pasting frequency

[a]Depending on the aluminium pasting frequency.

Thermal model

The typical process-of-records (POR) used in UBM/RDL production are reported in Figure 1 along with the simulated thermal profiles of a 300 mm Silicon wafer. Despite the tool configurations differ by the number of process chambers used, the process output in terms of (1) degas time and temperature, (2) etching amount and (3) PVD stack thickness remains the same. Based on the substrate properties, the thermal model calculates the heating rates of the different plasma processes involved, as well as the cooling rates during transfer and in-situ cooling provided by "arctic" etch and Ar backside gas. In the HEXAGON tool, the first process chamber in vacuum fulfills the role of cooling station. Here the substrate is mechanically clamped to the chilled pedestal for 50 sec. At the same time, Argon is applied at the wafer backside to increase the cooling efficiency. The combination of the cooling step and split etch approach results in a substrate temperature of 145°C (Figure 1a). On the other hand, the absence of the cooling station on the CLUSTERLINE® and the full etch amount performed in a single chamber result in a 40°C higher peak temperature (Figure 1b). In general, a lower temperature after the etching process is another beneficial aspect that helps to reduce outgassing and the related risk of recontamination, thus contributing to a better R_c control. The POR run on the HEXAGON results in a peak temperature of 170°C at a throughput of 54.5 wafers/hour. The CLUSTERLINE® POR reaches a peak temperature of 186°C and 33.3 wafers/hour throughput.

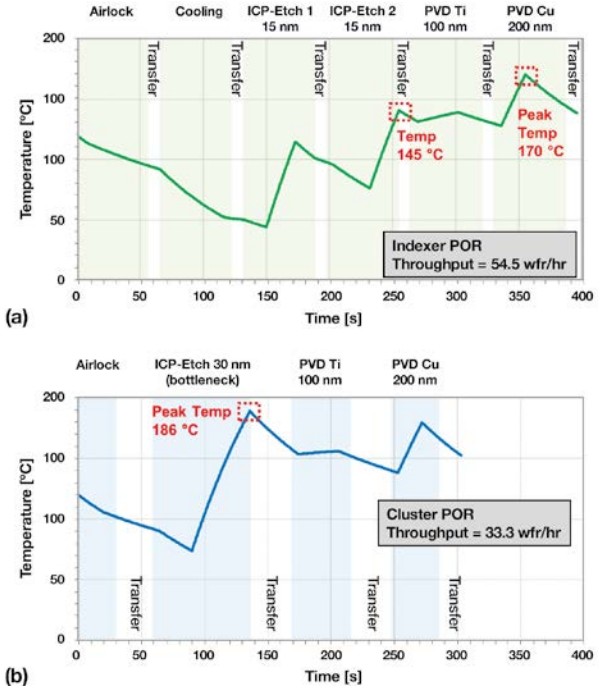


Figure 1a & 1b: Thermal profiles of a 300 mm Silicon wafer processed with UBM/RDL POR on the HEXAGON (a) and on the CLUSTERLINE® (b).

Wafer transfer in the HEXAGON

During process, the chamber pedestal is in the upper position and the cylindrical bellow fixated to the pedestal pushes the wafer carrier against the chamber flange. The isolation of the chamber is realized by compressing the two Viton seals inserted in the upper surfaces of the bellow and in the carrier against the above metal surfaces [12] (Figure 2 (a)). The transfer sequence is illustrated in Figure 2 (b)-(e). As soon as the bottleneck sequence is completed, the control SW issues the transfer command. The transfer sequence starts by the synchronized pneumatically driven down-stroke movement of all pedestals, which takes approximately 2.0 seconds. This action compresses the chamber bellows and consequently unseals the process environment in regard of the VTM. During the down movement, the wafers are placed on the carriers mounted on the HEXAGON carousel. The carousel plane is situated at an intermediate level between the two extreme positions of the pedestal. When the pedestals are in the lower position, the HEXAGON is free to move. At this moment, the servo motor drives in 3.0 sec the 60°-clockwise rotation of the carousel. As a result, all wafers are transferred simultaneously to the subsequent process station. It is important to note that during the indexing phase, process chambers and VTM share the same vacuum conditions. Next, the synchronized 2.0 sec up-stroke movement of the pedestals lifts the wafers from the carriers and seals again the chambers from the VTM. Now the wafers are sitting on the chuck top and the process sequence can start. In the new HEXAGON platform with central servo motor, the whole wafer transfer sequence takes approximately 8.0 sec. This is 5.0 sec faster compared to the earlier platform generation with a gear-driven carousel.

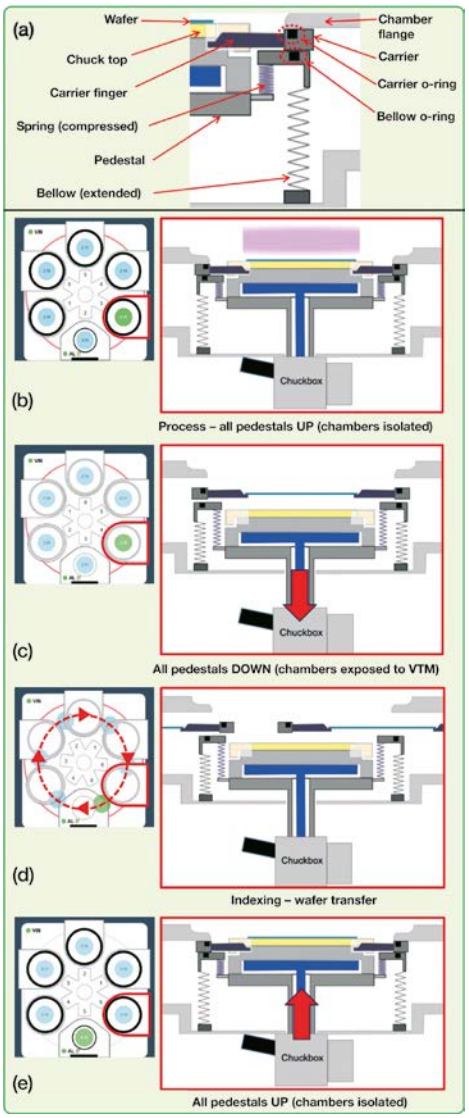


Figure 2: Chamber cross section (a) and wafer transport steps in the HEXAGON with central servo motor (b)-(e).

Wafer transfer in the CLUSTERLINE®

The transfer sequence in the CLUSTERLINE® is illustrated in Figure 3. Up to six process chambers and two airlock units are clustered around the VTM. The latter is equipped with a bisymmetric arm robot performing pick-&-place operation. All process stations and

airlocks are isolated from the VTM by means of individual slit valves. The valve opens prior wafer pick and closes after the next wafer has been placed. Thus, the VTM is exposed to the process chamber environment for a 15.0 sec time interval. The pedestal of the process chamber is actuated by a servo motor, and this is allowed to move only when the slit valve is closed. Both the down and up-stroke movements require approximately 10.0 sec. The total chamber-to-chamber transfer in the CLUSTERLINE® is approximately 30.0-35.0 sec. This corresponds also to the time interval between the end of the ICP sputter etch sequence (flow bottleneck) and the start of the Ti deposition. During steady-state operation, it can be observed that one wafer remains on standby on one of the robot arms until the ICP etch chamber becomes available (Figure 3 (a)). Since the wafer in question was previously degassed in the ABD, its temperature remains in the order of 100°C and thus continues to outgas and contaminate the VTM during its residence.

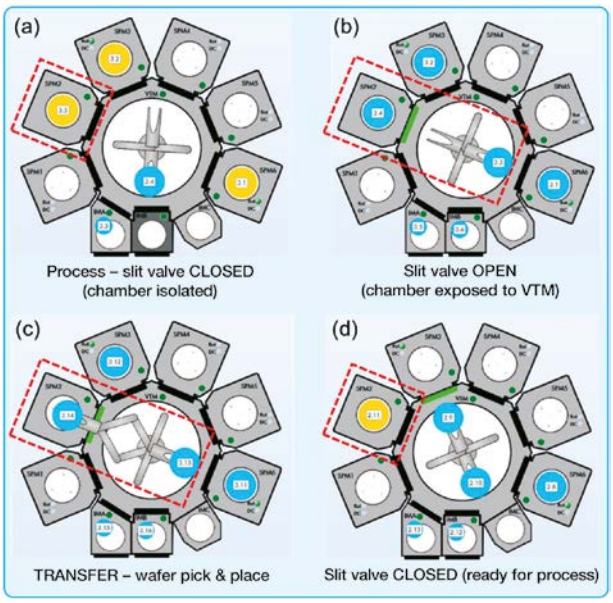


Figure 3: Wafer transport sequence in CLUSTERLINE® with bisymmetric-arm robot in the VTM. Each chamber is isolated from the VTM by means of individual slit valves.

Airlock cycle

Figure 4 compares the airlock performance of both systems. The pressure curves were recorded during a cycle run of SiO2 wafers. The pumpdown and venting time, as well as the wafer transfer time in vacuum and atmosphere are indicated. The reduced volume and the pumping scheme of the HEXAGON airlock are optimized for fast vent/pump cycle. Typically, the pumpdown time from atmosphere to the vacuum threshold 5.0E-5 Torr requires 10.0 sec. The venting time with N2 takes approximately 5.0 sec. During the movement of the airlock pedestal followed by the indexing, the pressure measured in the airlock is in the order of 1.0E-5 Torr, meaning two decades higher than the pressure of the VTM (not shown here). This different pressure level in regard of cross-contamination will be discussed in Section IV.

The control SW of the CLUSTERLINE® manages the operation of two airlock units in parallel. Each airlock has a capacity of two substrates. The upper position is reserved for the incoming substrates, which have been previously processed in the ABD. The lower position is reserved for the outcoming wafers, whose process is complete and are transferred back to the FOUP. The typical pumping time to the vacuum threshold of 5.0E-5 Torr is 25.0 sec and the venting time is 16.0 sec (Figure 4b). The slower pump and vent result in part from the larger airlock volume compared to the HEXAGON design. In the example shown, the base pressure of the airlock approaches 1.0E-5 Torr for a residence time of 40.0 sec. Then, as soon as the slit valve opens to allow the wafer transfer, the airlock pressure drops due to the lower pressure level of the VTM. During the indicated 14.0 sec necessary for placing the outgoing wafer and picking the incoming wafer, the VTM is to some extent exposed to the contamination from the residual atmosphere of the airlock.

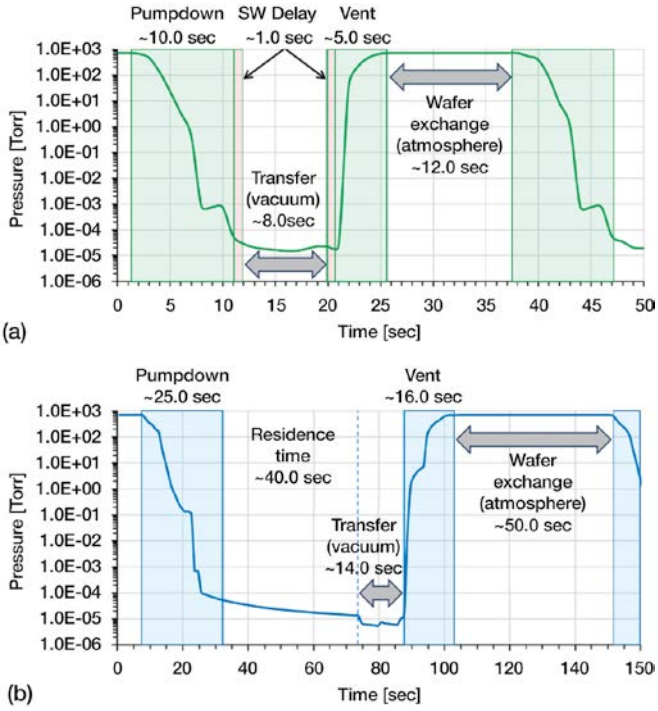


Figure 4a & 4b: Airlock pressure curves indicating pumping/venting and transfer time: HEXAGON (a) and CLUSTERLINE® (b). In both cases SiO_2 wafers were used.

Experimental Method

A series of tests is conducted on 300 mm wafers to characterize the contamination caused by the residual outgassing. RGA measurements are performed with HPQ3 model from MKS, whose upper working limit is 1.0E-3 Torr [13]. RGA devices are installed in two strategically important locations of the PVD platforms, namely the VTM and the Ti deposition chamber. Measurement in the VTM provides information on the outgassing propagating from the process chambers during the time interval when the wafers are in transit. Whereas data collected in the PVD-Ti chamber provides information on the background contamination before the start of the film deposition. Two different sets of wafers were used to execute the test plan summarized in Table II. A batch of 25 Si wafers with 5'000 Å of thermal oxide grown on both frontside and backside was used as a reference of non-outgassing material. A second lot of 25 Si wafers coated with 9.0 µm of PBO was used to mimic the outgassing of real products with organic passivation. RGA data of both wafer lots are presented in Section IV.

Design of Experiment – Datasets Collection

Platform	RGA location	Wafer type (25-wafers run)	
HEXAGON	VTM	SiO_2	PBO
	PVD-Ti	SiO_2	PBO
CLUSTERLINE®	VTM	SiO_2	PBO
	PVD-Ti	SiO_2	PBO

Figure 5 illustrates the system configuration, the locations of the RGA and the corresponding flow used to process the test wafers. Degas and ICP sputter etch processes were performed according to the POR previously described. In contrast, no metal was sputtered in the PVD chambers, instead the wafers were kept in vacuum for 50.0 sec. The RGA spectra were recorded from 1 to 50 a.m.u. during continuous wafer run.

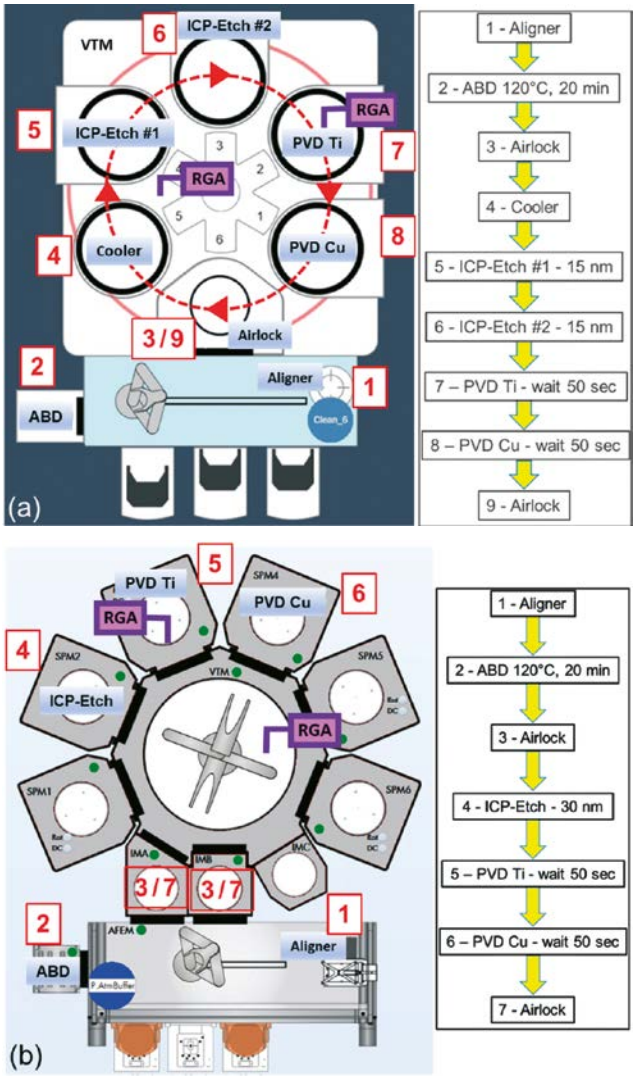


Figure 5: Configuration of the PVD systems used in HVM: HEXAGON (a) and CLUSTERLINE® (b). The process flows executed to run the cross-contamination tests are indicated beside each platform.

Results

Each dataset presented in the next paragraphs refers to a 25-wafers lot. To avoid a too clogged display, each chart is limited to a timespan of 300 sec, which is sufficient to describe accurately the behavior of the lot. The masses of the different species present in the spectra were identified based on available libraries [14]. The results are presented and discussed based on a selected group of the most prominent masses measured. These are in part originated from the Argon process gas, such as masses 40 and 20, which are attributed to Ar+ and Ar++. The other masses considered are related to the volatile contaminants. Masses 18, 17 and 16 can be attributed to the presence of water molecules (H2O+) and the corresponding fragments, i.e. HO+ and O+. However, mass 16 can also be related to the ion CH4+. The presence of organic contaminants is normally indicated by the species with mass 28 (CO+) and mass 44 (CO2+). The signal of mass 28 can also be attributed to nitrogen (N2+) as a specie present in the base pressure of the system and in the residual airlock atmosphere. Finally, mass 32, attributed to O2+, is also monitored.

HEXAGON – VTM RGA: SiO_2 vs. PBO Wafers

Figure 6 (a) and (b) displays the RGA spectra measured in the VTM of the HEXAGON during the process of SiO_2 and PBO wafers. The partial pressures of 4 known contaminants are compared in Table III. Masses 16 and 17 are omitted from the table as the former normally shows a marginal partial pressure and the second follows closely the trend of mass 18. Each of the pressure peaks, indicate that a transfer cycle takes place. At the instant t1 the pedestals move down to allow the rotation of the carousel. This event corresponds to a sharp increase of the VTM pressure. The contributors to this increase are: (1) the residual airlock atmosphere, (2) the residual Ar process gas, and (3) the volatile byproducts generated during the etching process. During transfer, at t > t1, the VTM pressure is mainly dominated by masses 40 and 20. In the case of PBO wafers, masses 28 and 40 are significantly more prominent than on SiO_2 wafers. This reflects the presence of byproducts generated during etching of this organic film. After transfer, the chambers are again isolated from the VTM environment. The pressure promptly recovers and stabilizes within seconds. At the instant t2 the Argon species practically disappear from the spectrum and the difference between the wafer types can be seen mainly by the higher partial pressure of masses 28 and 44. In both cases, at t3 the main contributors to the VTM pressure are masses 18 and 17.

The time interval between consecutive transfer events, e.g., t1 and t3, represents the wafer cycle time. When the cycle time is stable and constant, this can be used to calculate the steady-state throughput as indicated below:

$$Throughput = 3600/cycle\ time\ [\text{wafers/hour}] \quad (1)$$

The HEXAGON is running the process outlined in Figure 5a operates at a cycle time of 65.5 sec, which corresponds to a steady-state throughput of 55.0 wafers/hour.

CLUSTERLINE® – VTM RGA: SiO_2 vs. PBO Wafers

Figure 7a and 7b compare the RGA spectra measured in the VTM of the CLUSTERLINE® during the process of SiO_2 and PBO wafers. The partial pressures of the contaminants are reported in Table IV. The steady-state regime is reached when the process stations used by a given process flow are fully populated. This means, for instance, that the transfer history exhibits a periodic behavior throughout the job. In the steady-state conditions reached in this test, the vacuum robot necessitates 52 sec to transfer one-by-one the 5 wafers present in the system at once. The sudden pressure

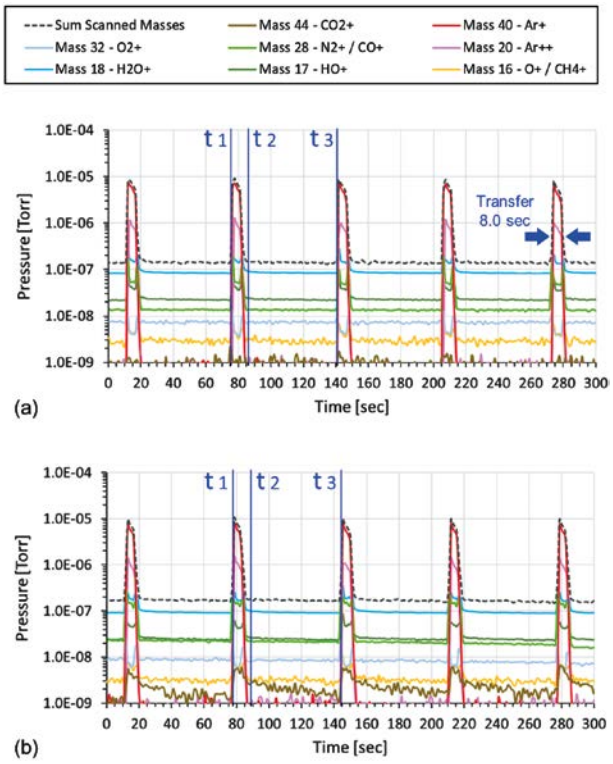


Figure 6: Selected masses measured in the VTM of the HEXAGON system, comparison of SiO_2 wafers (a) vs. PBO wafers (b).

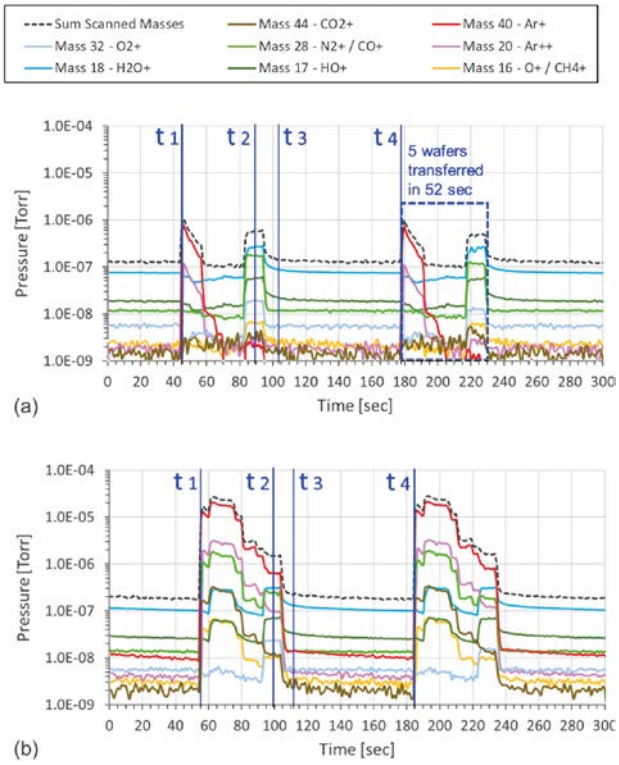


Figure 7: Selected masses measured in the CLUSTERLINE® VTM, comparison of SiO_2 wafers (a) vs. PBO wafers (b).

Time flag	Wafer type	Selected masses and partial pressures [Torr]			
		Mass 18	Mass 28	Mass 32	Mass 44
t_1	SiO_2	1.71E-7	5.76E-8	4.49E-9	9.56E-10
	PBO	2.5E-7	1.61E-7	7.75E-9	4.85E-9
t_2	SiO_2	9.6E-8	1.43E-8	7.3E-9	1.25E-9
	PBO	1.04E-7	2.24E-8	8.19E-9	2.79E-9

Partial Pressures of Contaminants (Data of Fig. 6)

Time flag	Wafer type	Selected masses and partial pressures [Torr]			
		Mass 18	Mass 28	Mass 32	Mass 44
t_1	SiO_2	6.64E-8	1.16E-8	2.6E-9	2.2E-9
	PBO	9.93E-8	1.07E-6	4.66E-9	1.64E-7
t_2	SiO_2	2.71E-7	1.74E-7	1.95E-8	4.22E-9
	PBO	3.12E-7	2.48E-7	2.28E-8	1.27E-8
t_3	SiO_2	9.2E-8	1.18E-8	5.04E-9	1.56E-9
	PBO	1.34E-7	1.39E-8	5.81E-9	2.38E-9

Partial Pressures of Contaminants (Data of Fig. 7)

increase observed at t1, corresponds to the opening of the slit valve of the ICP etch chamber to allow wafer picking. The residual outgassing load impacts the VTM pressure even after the etched wafer is placed to the next process chamber. Initially, in the case of SiO_2 wafers (Figure 7a) only masses 40 and 20 impact the VTM pressure. In contrast, on PBO wafers (Figure 7b) the total pressure is more than one order of magnitude higher and the contribution, beside Ar, comes from all other species, except of mass 32. At the instant t2, a wafer previously degassed in the ABD is picked from the airlock and enters the VTM. This action is accompanied by an increase of the partial pressures of mass 17 and 18, which is likely due to the outgassing of the hot wafer. Similarly, masses 28 and 32 also increase and this can be explained by the residual atmosphere of the airlock. The VTM pressure is again stable at the instant t3; however, there is a much more significant contribution of masses 40 and 20, and in a lesser extent of mass 44, in the case of PBO wafers. This phenomenon was not observed on the HEXAGON (Figure 7b). During steady-state operation, between t3 and t4, one wafer remains idle on the robot arm waiting to be placed in the ICP etch chamber. Since the temperature of this wafer is still around 100°C it continues to outgas and to contaminate the VTM environment. The periodic time interval between t1 and t4 can be used to calculate the steady-state throughput with (1). Thus, a cycle time of 128.7 sec corresponds to a throughput of 28.0 wafers/hour. The throughput limitation comes from the ICP etch sequence bottleneck summed to the overhead due to the chamber-to-chamber transfer.

HEXAGON - PVD-Ti chamber RGA: SiO_2 vs. PBO Wafers

Figure 8a and 8b compare the behavior of the PVD-Ti chamber of the HEXAGON during the residence of SiO_2 and PBO wafers previously processed with ABD, cooling step and split ICP etch. The instant t1, corresponds to the start of the down movement of the pedestal. This is accompanied by a sharp pressure increase caused by the volatile species coming from the other process chambers and by the residual atmosphere of the airlock. After the transfer, in the case of SiO_2 wafers, the total chamber pressure rapidly drops to the level indicated at t2 and remains stable until the next indexing event takes place at t4. Similarly, the contaminant species present remain constant during the timeframe t2-t4. On the other hand, one can notice a slow and steady decay of mass 40 in the same time interval.

In the case of PBO wafers, when the chamber is isolated from the VTM, such as at t2 and t3, the signal of mass 28 and 44 is almost one decade higher compared to SiO_2 (see Table V). Moreover, contrary to SiO_2, mass 40 remains the main contributor to the total pressure. The decay of mass 40 between t2 and t3, is somewhat slower compared to SiO_2. This may indicate that the film material itself and/or the surface roughness plays a role on the incorporation of Ar [15]. It is noteworthy to mention that mass 40 signal would completely disappear at t2 if no ICP etch process would have been performed, but instead only Ar gas would have been flown in the ICP etch chamber (data not shown here). This observation strongly supports the fact that Ar gets trapped in the film during the ICP etch process and is then gradually released over time.

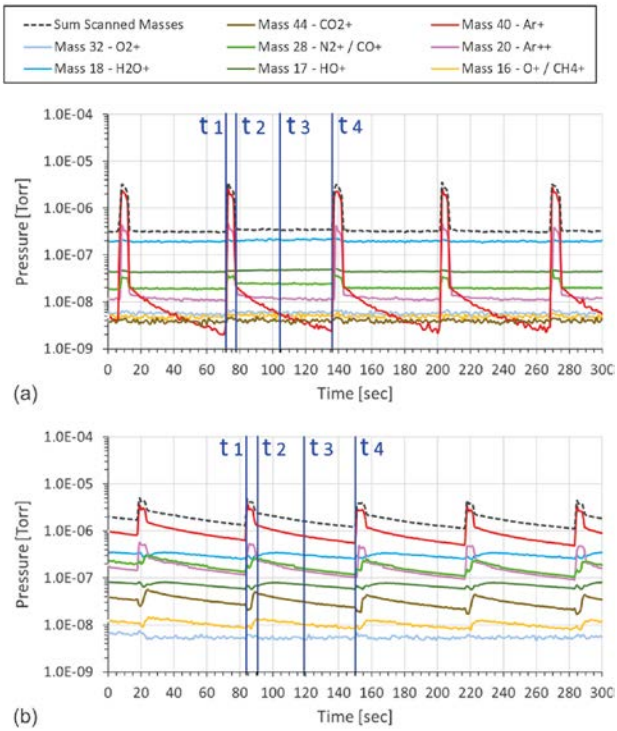


Figure 8: Selected masses measured in the PVD-Ti chamber of the HEXAGON, comparison of SiO_2 wafers (a) vs. PBO wafers (b).

Time flag	Wafer type	Selected masses and partial pressures [Torr]			
		Mass 18	Mass 28	Mass 32	Mass 44
t_1	SiO_2	2.11E-7	3.51E-8	6.66E-9	4.52E-9
	PBO	3.03E-7	1.86E-7	6.12E-9	2.12E-8
t_2	SiO_2	1.94E-7	2.59E-8	5.85E-9	4.45E-9
	PBO	2.96E-7	2.5E-7	5.9E-9	5.01E-8
t_3	SiO_2	2.12E-7	2.43E-8	5.71E-9	3.75E-9
	PBO	3.08E-7	1.55E-7	4.94E-9	2.99E-8

Partial Pressures of Contaminants (Data of Fig. 8)

CLUSTERLINE® – PVD-Ti chamber RGA: SiO_2 vs. PBO Wafers

Figure 9 (a) and (b) compare the RGA spectra measured in the PVD-Ti chamber of the CLUSTERLINE® during the residence of SiO_2 and PBO wafers. The typical base pressure level reached in PVD-Ti chamber reaches values in the low E-8 Torr. Due to the negligible outgassing of the SiO_2 material, when the chamber is isolated from the VTM, (i.e., starting at t1 until t < t4), the base pressure is barely affected by the wafer presence and remains below 5.0E-8 Torr (Figure 9a). The localized pressure instability observed between t1 and t2 is due to the movement of the pedestal from the hand-off position to the process position, which brings the wafer further away from the RGA device. Between t2 and t3, mass 40 exhibits a decay in a similar fashion as described earlier in Figure 8a. During the programmed 50.0 sec of waiting, the pedestal is in the upper position and wafer rests on the chuck top surface. In this so called "process position", the shields assembly restricts the pumping gap. As soon as the sequence time is elapsed, the pedestal moves to the hand-off position, where the pumping path opens and brings the wafer closer to the RGA. This explains the slight pressure increase starting at t3.

The residual outgassing measured on PBO coated wafers is obviously more pronounced compared to SiO_2 (Figure 9b). The total pressure remains to values above 3.0E-6 Torr during the entire residence time until t < t4. The dominating signals are masses 40 and 20, originated from Argon. These are followed, in descending

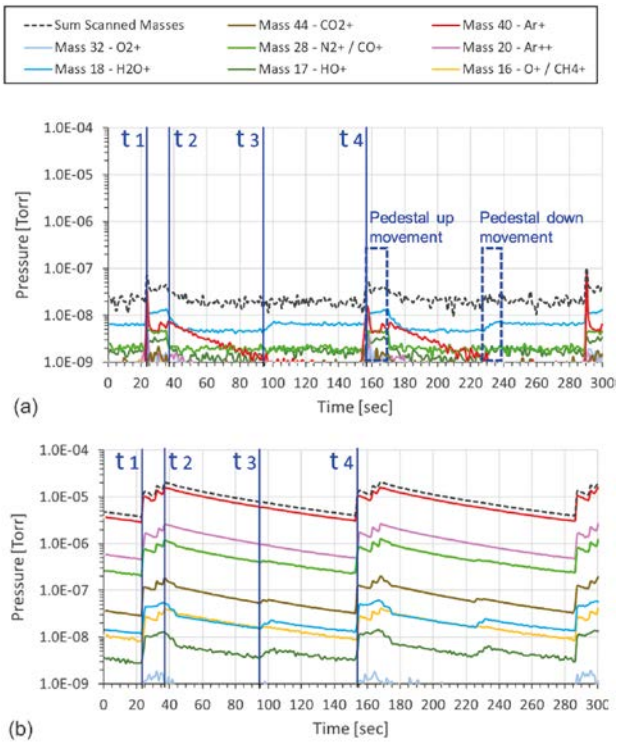


Figure 9: Selected masses measured in the CLUSTERLINE® PVD-Ti chamber, comparison of SiO_2 wafers (a) vs. PBO wafers (b).

Time flag	Wafer type	Selected masses and partial pressures [Torr]			
		Mass 18	Mass 28	Mass 32	Mass 44
t_1	SiO_2	1.23E-8	4.24E-9	1.16E-9	6.69E-10
	PBO	4.4E-8	7.64E-7	1.18E-9	1.17E-7
t_2	SiO_2	1.13E-8	2.37E-9	4.04E-10	8.46E-10
	PBO	5.25E-8	1.17E-6	1.1E-9	1.84E-7
t_3	SiO_2	5.71E-9	1.54E-9	2.38E-10	3.68E-10
	PBO	1.54E-8	3.98E-7	1.4E-10	5.48E-8

Partial Pressures of Contaminants (Data of Fig. 9)

order of partial pressures, by masses 28, 44, 18 and 17 (see Table VI). Similarly, to what observed on the HEXAGON, the rate of decay of masses 20 and 40 is somewhat slower on PBO than on SiO_2.

Summary

During steady-state operation, the VTM pressure of the CLUSTERLINE® is more severely impacted by the outgassing load propagating from the ICP etch chamber and from the etched wafer. This is particularly evident in the case of PBO, where the level of contaminants, especially masses 28 (CO+) and 44 (CO2+), is almost two orders of magnitude larger compared to the HEXAGON tool. Because of the longer chamber-to-chamber transfer interval on the CLUSTERLINE®, the etched wafer may incur in a higher risk of re-contamination from its own residual outgassing. In contrast, the faster and simultaneous wafer transfer in the HEXAGON allows the VTM pressure to recover almost immediately. In this platform, the wafer type plays a less prominent role as indicated by the minor difference in the level of contaminants measured on SiO_2 and PBO.

RGA data from the PVD-Ti chambers of both platforms have shown a very different behavior on SiO_2 and PBO. In general, the contamination caused by SiO_2 wafers is almost entirely due to masses 40 (Ar+) and 20 (Ar++). In the case of PBO wafers, the overwhelming contribution to the total pressure is as well due to masses 40 and 20, but the other contaminants are also present in a significant extent. One interesting difference is that the partial pressure of mass 40 in the CLUSTERLINE® is of order 1.0E-5 Torr, whereas in the HEXAGON it is one decade lower. Some other differences in the magnitude of the volatile contaminants can be distinguished, such as the 50% higher partial pressure of mass 28 (CO+) and mass 44 (CO+) in the CLUSTERLINE® chamber. A possible explanation is the higher wafer temperature reached during the single-step etching process performed on the ICP etch chamber of the CLUSTERLINE®, that in turn causes stronger outgassing in the PVD-Ti chamber. On the other hand, mass 18 (H2O+) exhibits one decade lower partial pressure in the chamber of the CLUSTERLINE®. This significant difference may be explained by the increased efficiency in the pumping of water molecules with the cryo pump, instead of the turbomolecular pump installed on the process chambers of the HEXAGON. The partial pressure of mass 32 (O2+), is situated at approximately 1.0E-8 Torr in the HEXAGON and is not affected by the presence of the wafer in the chamber. Mass 32 is one decade lower in the CLUSTERLINE® chamber. This is in line with the better base pressure conditions.

Conclusion

A quantitative RGA benchmark between the HEXAGON and the CLUSTERLINE® would not be fair due to important HW differences, such as chamber volume, pumping efficiency (cryo vs. turbo in the PVD chambers) and the physical distance between the wafer path and the RGA device. Nevertheless, RGA measured in the vacuum transport module and the PVD-Ti chamber have provided a good picture of the cross-contamination dynamics established during steady-state operation. Experimental data has clearly shown that the main source of contamination in both systems is the residual outgassing load of the etched PBO wafer, that migrates from the etching chamber to the VTM and then accompanies the wafer to the PVD-Ti chamber. Such argument is supported by the very different behavior observed on SiO_2 and PBO films. The former does not exhibit any residual outgassing due to volatile organic contaminants.

A common phenomenon observed in both platforms is the overwhelming presence of masses 40 and 20 in the cloud of volatiles species. This may indicate that a significant amount of Argon becomes trapped in the films as a side-effect of the ICP sputter etch process. During transfer and residence in the PVD-Ti chambers, Argon is then gradually released at a different rate depending on the film material. Although the scale of the Argon presence is very significant, the investigation of the root-cause of this phenomenon is beyond the scope of this paper.

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Productivity Boost and Optimum R_c Control in Wafer-Level Packaging enabled by HEXAGON

The megatrend of more miniaturized electronic devices highlights the importance of low and stable contact resistance (R_c). To classify the capability of HEXAGON as High-Throughput UBM/RDL Technology, we report the details of experimental work on throughput and R_c previously presented and published at ECTC 2023 by Evatec's ***Dr. Carl Drechsel***, ***Dr. Patrick Carazzetti***, ***Carl Wang***, ***Dr. Juergen Weichart*** and ***Ewald Strolz***, as well as ***Kay Viehweger*** from Fraunhofer IZM-ASSID (Moritzburg, Germany)[1].

INTRODUCTION

An impressive attribute of the digital transformation are the continuously growing amounts of data being processed. While the average monthly data volume per stationary broadband connection in Germany was only 47 GB in 2015, it had risen to 142 GB in 2019. In 2023 it was already 287 GB, which is about 10 GB per day. However, this does not include the mobile data volume, which averaged 7.2 GB per month in 2023 [2] and might increase tremendously in near future. Although these values differ considerably from country to country, there is nevertheless a clear global trend, which shows the requirement of data capacities that exceed our current average consumption by far: Operating an autonomous vehicle generates for example a data volume of around 5 GB per minute, which would amount to around 7.2 TB (= 7200 GB) per day. And if you want to estimate the amount of data being processed in a Smart Factory, you need to familiarize yourself with dimensions like Petabyte (1 PB = 10^6 GB) or Exabyte (1 EB = 10^9 GB).

The demand for higher data volumes goes hand in hand with a continuous trend for higher performance devices, increasing power efficiency and miniaturization. Recent progress is here explicitly based on wafer-level packaging (WLP) [3], where typically protective layers, electrical connections as well as the packaging itself are implemented before dicing the wafer into single chips. Hence, resulting packages are in similar dimension as the die itself, which is understood as wafer level chip-scale packaging (WLCSP). In advanced packaging this requires multi-layer and fine pitch packaging designs that push the dimensions of vertical interconnects and redistribution layer (RDL) technologies below 5 µm. But since smaller interconnects critically complicate the electrical performance requirements, the control of a low contact resistance (R_c) is becoming more and more important. Additionally, smaller scaling is in state-of-the-art packaging platforms coupled with higher organic loads that needs to be avoided, such as organic or oxide contamination of the metal interfaces.

Here we review hardware improvements that facilitate low R_c results (< 2.0 mOhm) on HEXAGON used in WLP for the creation of under bump metallization (UBM) and RDL. Keeping a low R_c, it is possible to reach a throughput of 80 wafers/hour (WPH). Key drivers for this optimization are an improved airlock design that effectively shrinks pumping and venting times, resulting in a cycle time of approx. 34 seconds per wafer. This allows other processes to be trimmed. Additionally, a new indexer rotation concept of the HEXAGON shortens the chamber-to-chamber transfer, which reduces the risk to re-contaminate the contact pads at the end of the ICP sputter etch step. The electrical performance relevant for R_c calculation is measured on single-contact Kelvin resistors with via diameters from 25 down to 10 micrometers. Experimental data show for all via diameters stable R_c results within a lot of 25 wafers at a high-throughput run of 80 WPH.


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I. EXPERIMENTAL METHODS

A. Overview on HEXAGON

To process the wafers, on which later the R_c is evaluated, a high-volume manufacturing HEXAGON platform, especially optimized for boosting the wafer handling speed, has been used. Figure 1 shows the configuration of the HEXAGON system.

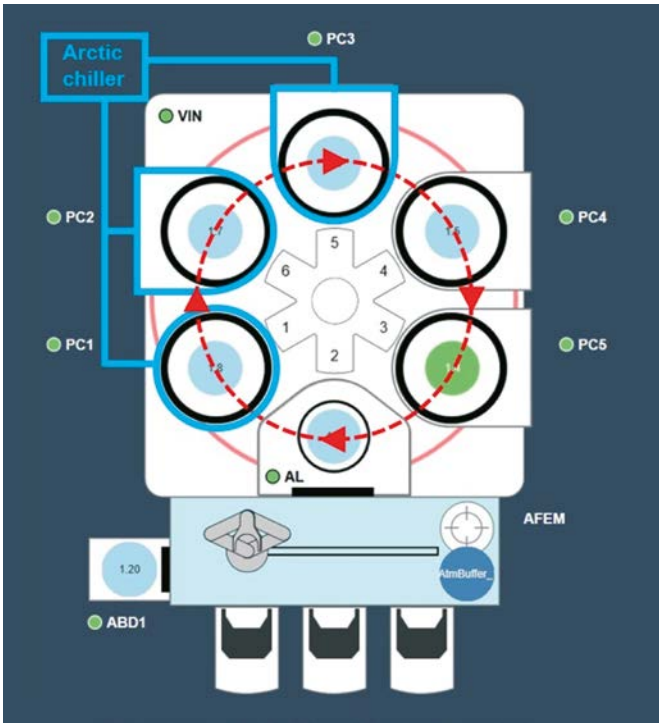

Figure 1: Configuration of HEXAGON platform, indicating pre-treatment (ABD, PC1, PC2, PC3) and PVD (PC4, PC5) modules.

The HEXAGON platform consists of two major components: An atmospheric front-end module (AFEM) and a vacuum indexer module (VIN). The AFEM is equipped with three loadport modules (LPMs) to introduce front opening unified pods (FOUPs) to the system, an aligner to correct eccentricity for every incoming wafer, a buffer as deposit place for pasting wafers and an atmospheric batch degasser (ABD). The VIN is equipped with an airlock (AL) to introduce wafers from AFEM and five process chambers (PCs). PC1 is an arctic cooling station to reduce the wafer temperature between ABD and the two inductively coupled plasma (ICP) sputter etch modules in PC2 and PC3. The ICP sputter etch procedure relies on physical bombardment with Ar+ ions in an ignited Ar plasma. Since ICP sputter etch processes are very critical to the thermal budget, the pedestal and the chamber shields are actively cooled to -30 °C by an external chiller unit. In PC4 and PC5 the PVD process of Ti as adhesion and Cu as seed layer for a final downstream process is performed.

B. Process Description

The procedure of the entire process, performed as BKM on single wafers, is described in Table I. Following the BKM, every wafer is first aligned and next transferred into the ABD, where a degassing phase takes place to avoid adsorbed water molecules on the wafer. There, a batch of 28 wafers can be processed simultaneously while a laminar N2 flow guarantees constant peak temperatures on the

Module	Physical process
LPM	FOUP is loaded to the AFEM & Wafer is taken
Aligner	Eccentricity check & notch alignment
ABD	20-30 min degassing at 120-130 °C
AL	Wafer is transferred from AFEM to VIN
PC1	Cooling to ≈ 50 % of ABD temperature
PC2	15 nm removal by ICP sputter etch
PC3	15 nm removal by ICP sputter etch
PC4	100 nm Ti PVD
PC5	300 nm Cu PVD
AL	Wafer is transferred from VIN to AFEM
LPM	Wafer is put back & FOUP is unloaded from AFEM

Table 1: Overview of BKM process flow

wafers, independently of the position and the total number of wafers loaded. The total degassing time and temperature is product specific and typically ranges 20-30 minutes and 120-130 °C. After degassing, wafers are transferred to the AL and thus get into the VIN. Next, they enter the first process chamber (PC1) and cool down to roughly half of the ABD peak temperature. This is important to ensure that the thermal budget of the ICP sputter etch process in PC2 and PC3 starts from a preferably low point. Since etching gives the highest amount to the thermal heat on the substrate, the total etch amount required is equally distributed to PC2 and PC3. In addition to pure Ar+ ion bombardment, the entire etching process also includes in-situ cooling and purging steps to reduce the peak temperature. After finishing the etching and the Ti/Cu PVD in PC4 and PC5, the wafers get back to AL and are therefrom re-transferred to the FOUP.

C. R_c Measurement

The R_c measurements are performed on four-terminal Kelvin resistors, built on 300 mm Si wafers. An overview of all steps necessary for the completion of a full R_c test vehicle is illustrated in Figure 2.

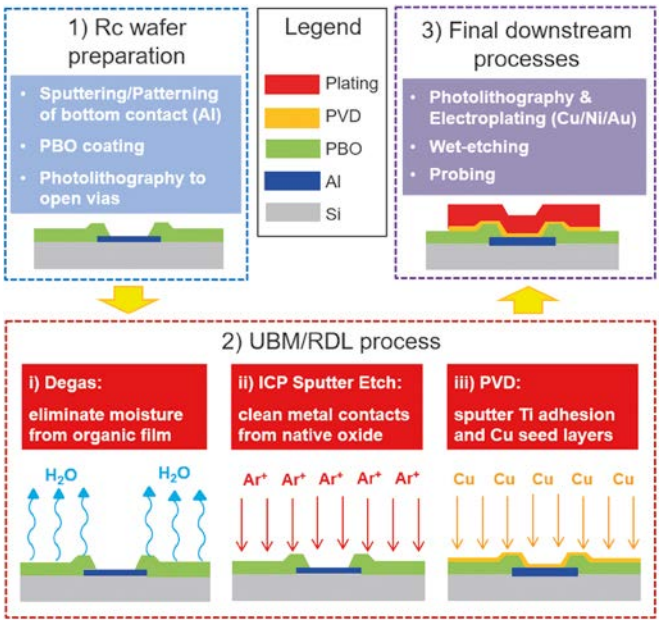

Figure 2: Fabrication flow indicating process steps of Rc test vehicles on 300 nm Si wafers.

Each R_c test vehicle consists of a patterned metallization layer (1 µm sputter-deposited Al) on a Si substrate, which acts as basic redistribution line (RDL0). On top of that a 9 µm thick passivation film of PBO is deposited. By means of photolithography, a contact opening via is created on top of the RDL0 (see Figure 2, step 1). The smaller the diameter of the opening pad d0, the more sensitive to the R_c is the Kelvin resistor. This is followed by the BKM flow (see Figure 2, step 2). Cleaning the pads and depositing Cu as RDL1 without oxidation is essential for an optimum operation of the device and is revealed by a low Rc. Next the final downstream process follows, which includes a thickening of RDL1 by 3 µm Cu electroplating and an addition of 2 µm Ni and 0.5 µm Au by selective plating of the probing pads to improve the reliability of the latter R_c measurement (see Figure 2, step 3).

An enlargement of a test vehicle used for this study and a sketched cross section of an opening via is shown in Figure 3. Each test vehicle has a total number of 121 cells, containing series of Kelvin structures differing in via diameter (d0), overlap size between RDL0 and RDL1 that is equal to 0.5(d1 – d0) and connector width c. The R_c measurement is performed at a voltage in the order of 1 mV with a vertical probe card. It is leveled by a fully automatic probe station (TEL Precio) and the high-precision measurement is conducted by an Advantest V93k test head with analog VI cards. A detailed description of the measurement procedure and calculation of the R_c can be found in [4].

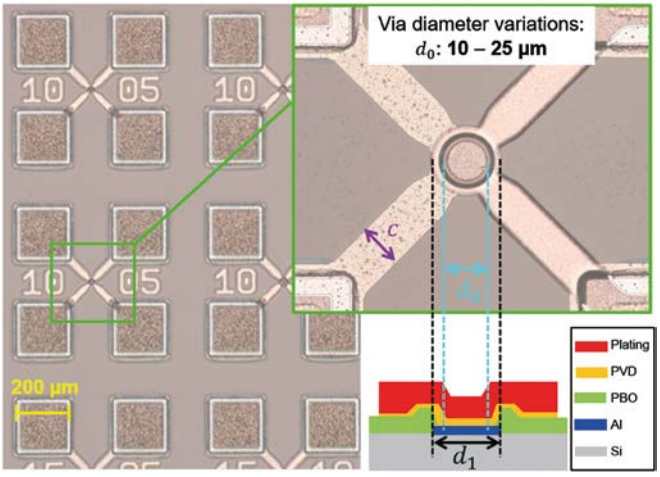

Figure 3. Enlargement of Rc test vehicle with four-terminal Kelvin resistors

As standard qualification procedure, for each experiment condition, a lot of 25 wafers is processed with the described BKM. Before the lot is started, a single Al pasting wafer is etched for 90 s to ensure similar conditions in PC2 and PC3. PC4 and PC5 are warmed up with PVD processes on 4 dummy wafers. In the lot, the R_c test vehicles are located in slots 1, 13 and 25, while all other slots are filled with PBO dummy wafers.

II. HARDWARE FEATURES OF HEXAGON

The optimized, high throughput of HEXAGON is the consequence of a very short cycle times. The cycle time itself can be divided into handling time and process time.

The handling time denotes the duration a PVD system needs to transfer all wafers to the next process chamber between completion of the last process and start of the next process. In an indexer system, it consists of a synchronized downward pedestal movement, a 60° clockwise rotation of the indexer carousel and an upward pedestal movement.

The process time is product specific and depends mostly on the required etch amount and PVD thicknesses. However, in standard applications of UBM/RDL deposition, the etching sequence is usually the process time bottleneck. Within the ICP sputter etch sequence, there is also time for pumping and purging before and after pure etching in order to prevent contamination of the etched pads and to keep the thermal excursion as low as possible.

A. Optimized Indexer Unit

The reduced handling time of HEXAGON has its origin in the design of the central rotating device. While in previous indexer systems the support paddles on the indexer carousel were connected to a motor by gears (see Figure 4a), the new design places the paddles directly on the rotary table driven by a central servo motor (see Figure 4b). Only this causes a time gain of approx. 2 s. Additionally, the potentially higher attrition of the gear wheel components is counteracted. The total handling time was shortened to approx. 9 s.

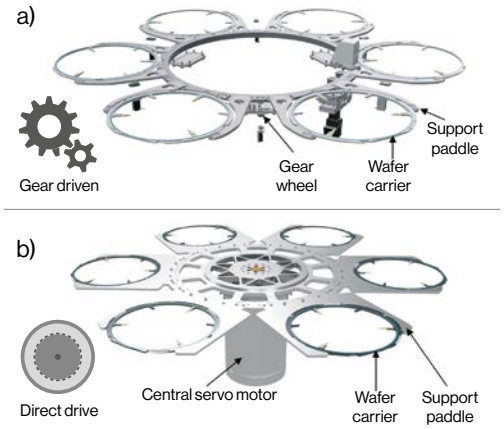

Figure 4. Comparison between previous and new design of central rotating device; a) previous gear driven indexer unit; b) new direct drive approach.

B. Optimized Airlock Cycle

HEXAGON also uses an optimized AL design. Compared to an earlier indexer tool design, the AL volume V0 has been reduced to 25%. Instead of one large turbo pump, two smaller ones, each with its own pump valve, are installed (see Figure 5).

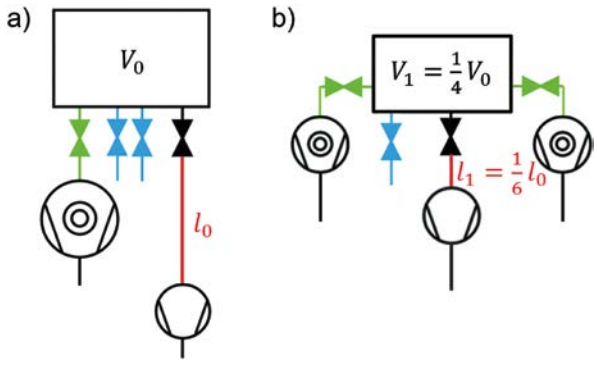

Figure 5. Scheme of AL in a) previous design and b) new design. Different colors indicate pumping valves (green), venting valves (blue) and fore-vacuum valves (black). The pumping line to fore-vacuum pump is marked in red.

Furthermore, the pump line l0 between the fore-vacuum valve and the roughing pump was shortened by mounting the roughing pumps directly on the main frame of the tool. All in all, this enabled the pumping time to be roughly halved. The number of venting valves at the AL has been reduced from 2 to 1, since the reduction of the AL volume does not require more venting capacity. Even so, the venting time at AL is also reduced by about half.

By the optimization of AL, a cycle time of approx. 34 s can be reached, which corresponds to a peak throughput of approx. 105 WPH when the system runs in dry-cycle mode. A pressure-time analysis of the AL, including pumping, handling time, venting and wafer exchange is illustrated in Figure 6.

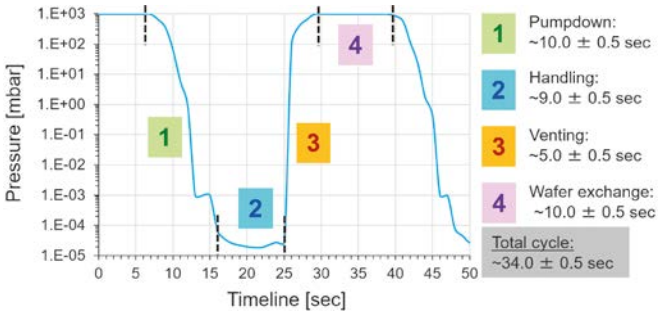

Figure 6. Pressure vs. time analysis of a single AL cycle time.

III. THERMAL MODEL AND R_c ANALYSIS

A. Thermal Model

The temperature flow over the whole BKM stack can be simulated with a thermal model [5]. Applying it to throughputs of 44.2, 54.5, 69.2 and 80.3 WPH (see Figure 7), allows to determine the peak temperature after ICP sputter etch process and over the full stack process. From this, a correlation between peak temperatures and the respective throughput can be determined (see Figure 8).

B. R_c Analysis

For all throughputs, on which the thermal model is applied, the R_c is measured on a lot of 25 wafers. It indicates on which values and how constant the R_c remains in the face of higher chamber temperatures during continuous operation. Figure 9 shows for different throughputs the averaged result for via diameters of 10, 15, 20 and 25 µm on wafers in slots W#1, W#13 and W#25.

All R_c results for investigated throughputs are in the order of 1-2 mΩ. Only the run at 44.2 WPH shows higher values at a via diameter of 10 µm for wafers #13 and #25. Regarding to the examined via diameters, a larger diameter generally leads to lower R_c values. Within a FOUP, the R_c values remain extremely stable at 80.3 WPH, while a slight increase can be observed at 69.2 WPH and a significant increase at 44.2 WPH. For 54.5 WPH the R_c values even decrease very slightly. The statistical error ranges are very small for the measurements with via diameters of 20 and 25 µm, for 15 µm they are a bit larger. For 10 µm, on the other hand, the error ranges are more than twice as large. This arises from the systematically more inaccurate measurement conditions for smaller via diameters.

Overall, the R_c results for high-throughput runs on HEXAGON reach a very low level (< 2 mΩ). Although the peak temperature is highest at 80.3 WPH (see Figure 9), no negative impact on the R_c behavior can be detected, which is attributed to faster process and handling times, reducing the potential time for a recontamination of the etched pads.

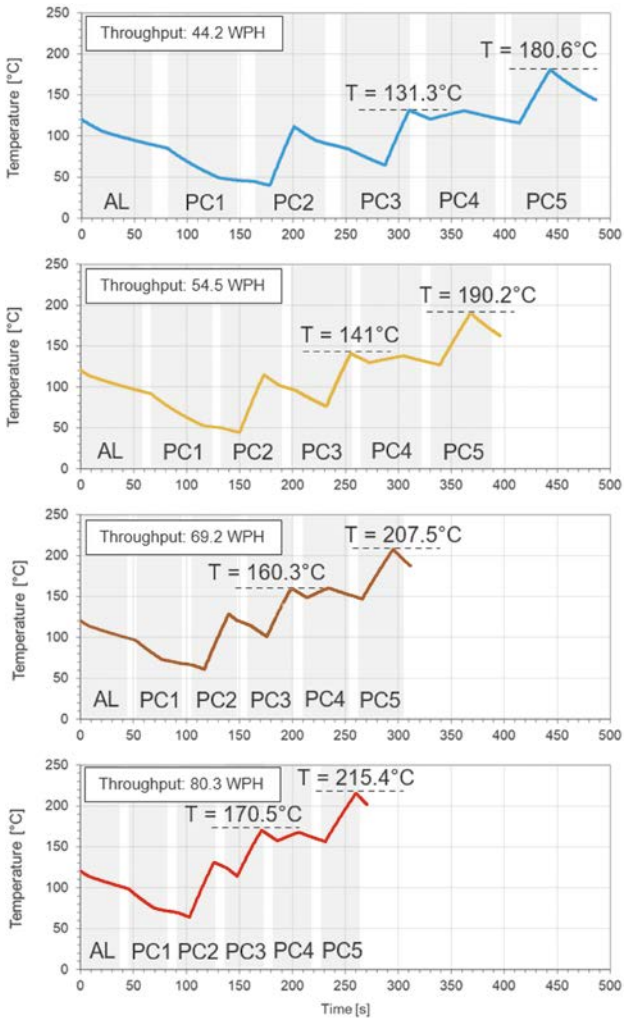

Figure 7. Thermal model for different throughputs, indicating the maximum temperature after ICP sputter etch and for the entire process.

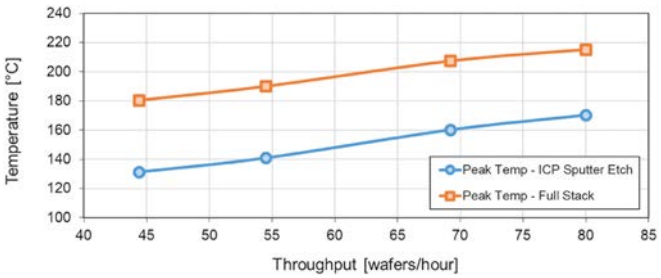

Figure 8. Peak temperatures after ICP sputter etch process and within total stack for different throughputs.

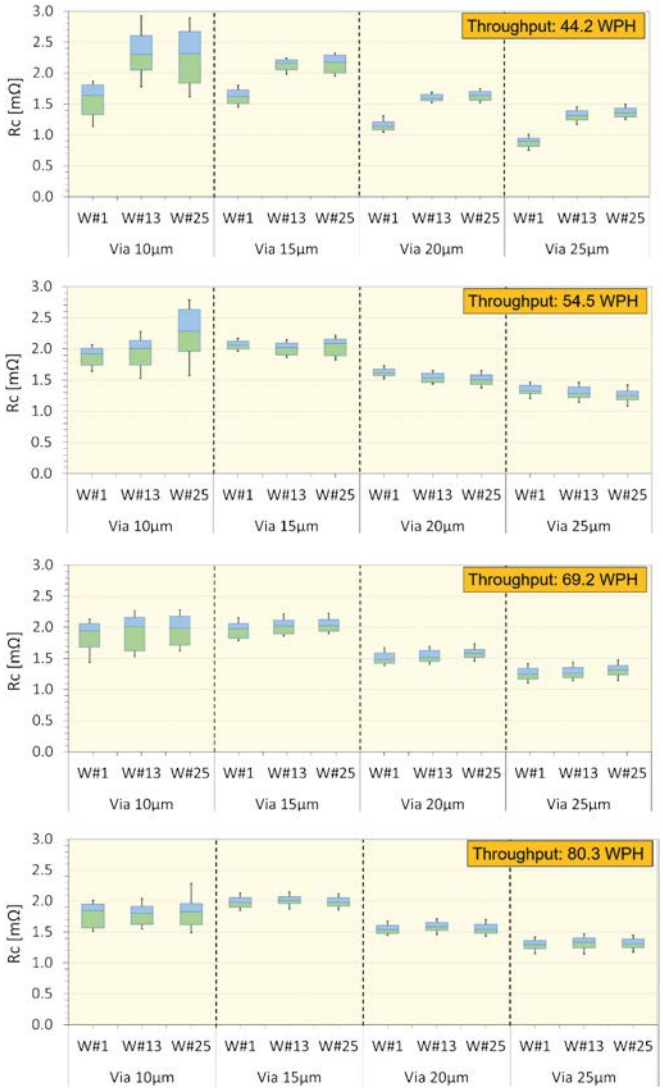

Figure 9. Rc results for different throughputs and via diameters. W#1, W#13 & W#25 indicating the slot position of the test wafer within a FOUP.

CONCLUSION

Due to continuous miniaturization in high-end and advanced packaging, the control of R_c has uttermost importance. In this work we discussed the achievement of low R_c results on a HEXAGON system used for UBM/RDL in WLP. At the same time, the throughput is increased to 80 WPH based on hardware improvements.

The hardware optimization can be divided into a new design of the central rotating device and the AL. The first leads to a reduction of the handling time, the second leads to a reduction of the AL cycle time, i.e. the duration the AL needs to pump down, handle, vent and exchange a wafer. Based on experimental data, the R_c was measured for throughputs between 44.2 and 80.3 WPH on single-contact Kelvin resistors with via diameters of 25 down to 10 µm, located in the 1st, 13th and 25th slot of a FOUP. Furthermore, the temperature profile of a test wafer was simulated for all throughputs, from which the peak temperature after etching process and for the full stack process is determined.

It could be proven that an increase in throughput is associated with an increase of the peak temperatures, but at the same time no increase in R_c is observable. In particular, the via diameters of 10 and 15 µm show a lower R_c at high throughput. The comparison of the R_c results for the 1st, 13th and 25th wafer exhibits no increase for wafers within one full lot. In summary, we provide evidence that an increase in throughput on a HEXAGON platform goes hand in hand with an optimum R_c control. This performance is achieved even though the full stack peak temperature exceeds 215 °C.

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Advances in Frontside Process Technology: Trench/Via Filling & Planarization

Trends in frontside contact formation in new power device technologies on Si or SiC are calling for ever more demanding thin film processes – trenches get deeper, aspect ratios get higher and expectations for the quality of the final planarized surface grow. Evatec's Product Marketing Manager ***Fabian Kramer*** and Manager of Technology Development ***Mohamed Elghazzali*** give us a taste of the Evatec solutions supporting customers in 2025 and beyond.

The process requirements are clear

Trench/Via filling and planarization processes call for deposition of two layers.

1. A "seed" layer with good step coverage – typically comprising a thin titanium layer in the range 20-50 nm followed by a TiN layer in the range 150-250nm. The Ti layer acts as adhesion layer and TiN as barrier layer.
2. A thick metal contact layer, typically Al , AlCu or AlSiCu according to the device design in the thickness range between 3000-5000nm. The process conditions need to ensure good flow of the material within the trench without voids and provide good final planarization.

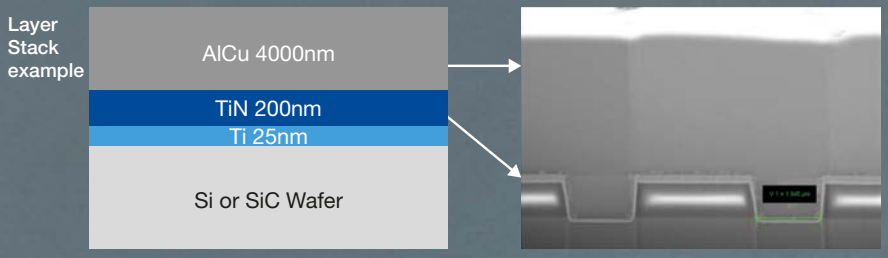
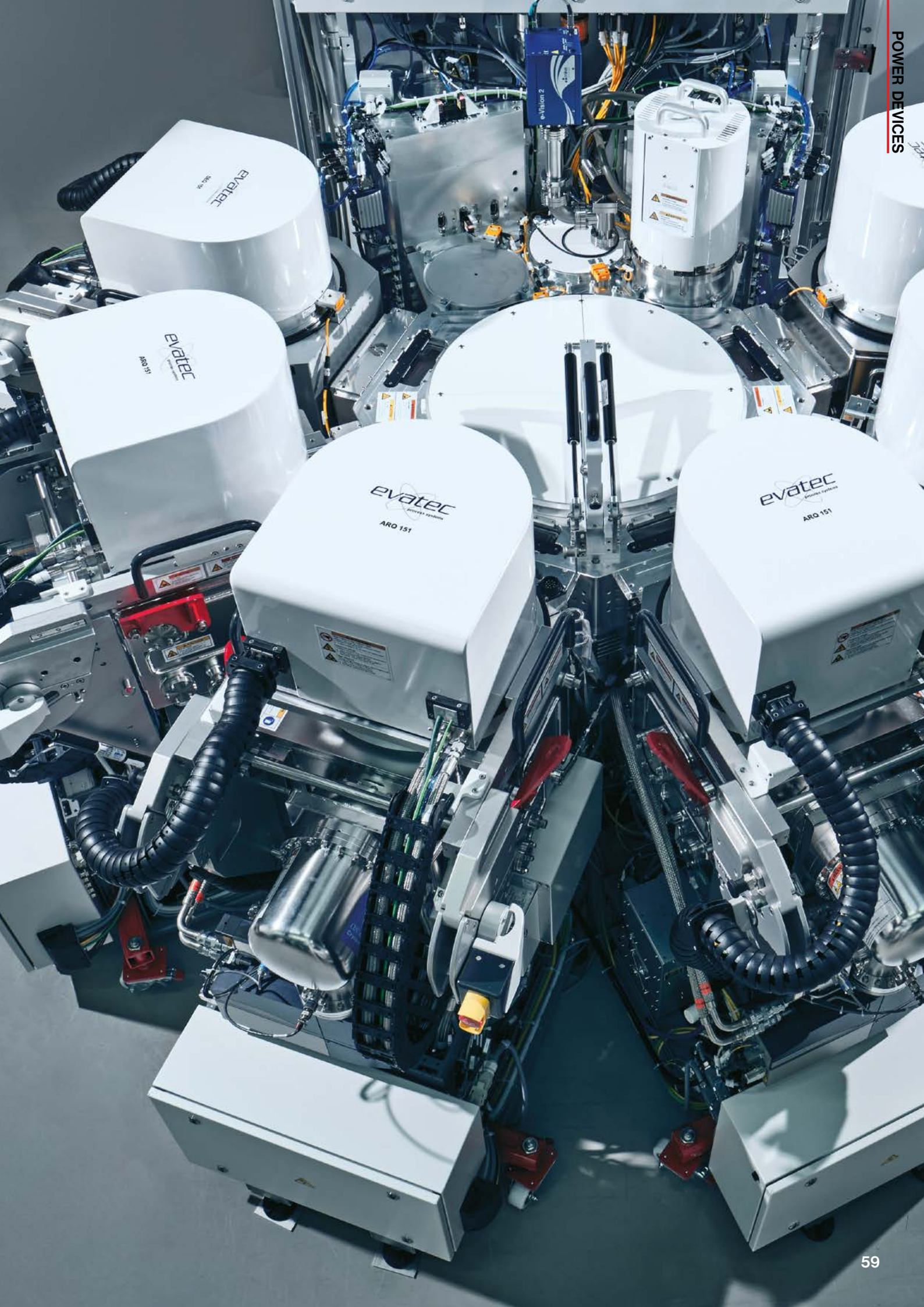


Figure 1: CLUSTERLINE® 200 results for trench filling and planarization

"Supporting Perfect Al Flow in higher aspect ratio trenches"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CLUSTERLINE® solutions are already well established

Evatec's CLUSTERLINE® 200 and 300 platforms are already well established in power device applications.

Figure 1 illustrates a micrograph of typical results achieved on CLUSTERLINE® 200 for frontside contact formation with trenches of aspect ratio approximately 1:1. Seed layers provide the step coverage required for good aluminium adhesion, while good material flow at process temperatures around 400ºC provides the required void-free films with smooth surfaces. Details of a typical single process module are shown in Figure 2.

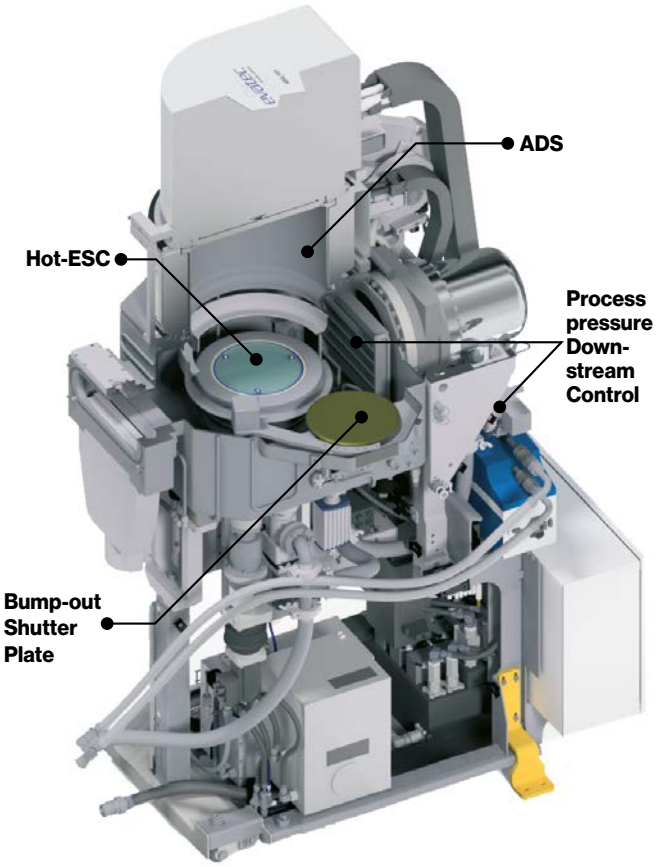


Figure 2: Single process module

More challenging process demands are coming in 2025

Emerging trends in device architecture calling for higher aspect ratios are setting more demanding challenges for substrate handling and thin film processes.

Seed layer deposition needs to achieve sufficient side wall and bottom coverage without significant increase in overall film thickness. For the thick metal layer deposition, substrate handling within the process chamber needs to avoid "sticking" and the risks of subsequent damage or particle generation, while Al Flow still needs to ensure void free films for the more demanding device architectures.

New solution to achieve a higher aspect ration of 3:1

New dedicated hardware and process control features being introduced to the market at the end of 2024 for CLUSTERLINE® 200 will enable our customer to achieve the new levels of process performance for high aspect ratio features.

- Enhanced new module design for Advanced Directional Sputtering (ADS) will deliver the improved step coverage essential for higher aspect ratio trenches without increasing required TiN film thickness and deposition times.
- Process module control technology leveraging downstream pressure control will deliver enhanced process control and process repeatability for the reactive processes required in TiN deposition for the most consistent seed layer deposition in higher aspect ratio applications
- New process kits including integrated substrate shutters and modified shielding will bring further benefits:
  - Elimination of any wafer pasting steps required simplifying processes and increasing wafer throughput
  - Improved particle management
- New full face Electrostatic Chuck (ESC) for efficient thermal coupling will enable process temperatures up to 500ºC, which will offer customers wider process windows for any new processes and reduce risk of wafer sticking and edge damage.

CLUSTERLINE® 200 is the solution

CLUSTERLINE® 200 enables integration of up to 6 process modules. A possible system layout for front side contact metallization integrating these new capabilities is shown in Figure 3.

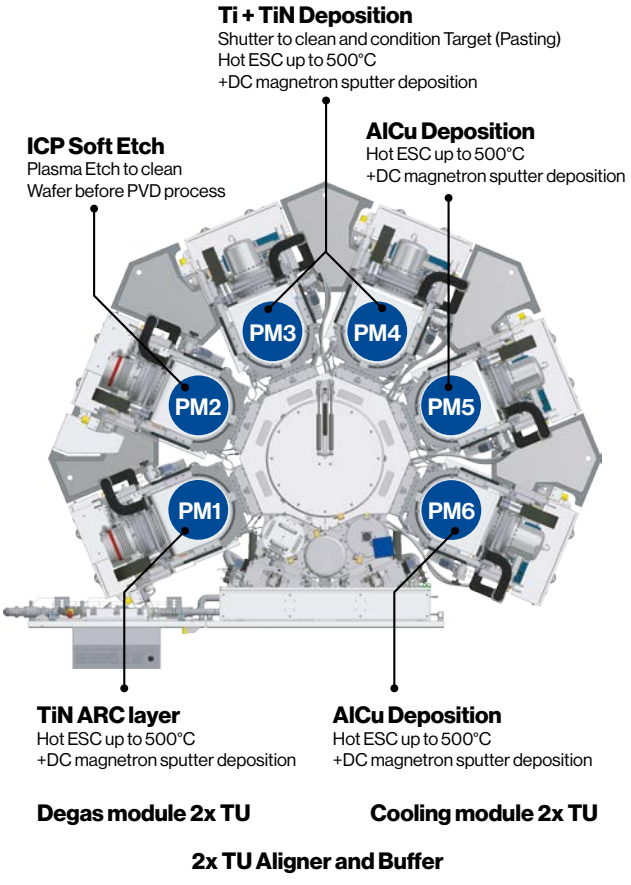


Figure 3: Typical CLUSTERLINE® 200 configuartion for gap filling and planarization

SPOTLIGHT ...CLUSTERLINE® 200

A choice of architectures

The CLUSTERLINE® 200 can be configured as a tool for single substrate or batch processing using Single Process Modules (SPM) or a Batch Process Module (BPM) respectively. However, when you configure the tool, you can rely on fully automated cassette-to-cassette processing using Evatec's proven safe handling. For custom applications please also enquire about configurations combining both single and batch process modules.

SPM configuration highlights

Platform variant with strong pedigree in Power Devices, Advanced Packaging, MEMS and Wireless markets allowing easy tool configuration and future expansion for PVD, highly ionized PVD, Soft Etch, PECVD and PEALD for wafer sizes up to 200mm.

- Modular chuck design for rapid exchange between 100, 150 or 200mm formats for production flexibility and maximum tool utilization
- Up to 6 single process modules and up to 6 auxiliary modules for pre- and post treatment steps
- Auxiliary module functions including wafer alignment, buffer, degas, cooling, and ID reader
- Direct thin wafer handling and processing capability for substrate thicknesses down to 70 microns

BPM configuration highlights

Platform variant combining the benefits of sputter batch processing with completely automated handling for selected applications in MEMS and Wireless. A true work horse in the LED / Micro Display and Photonics industries. Integration of additional plasma sources opens up process possibilities for enhanced deposition processes e.g. coating modification including gap filling and planarization.

- Batch processing of up to 20+1 six inch substrates simultaneously
- Batch processing of up to 15+1 eight inch substrates simultaneously
- Rotating substrate table with option for individual rotating substrate chucks
- Integration of up to 4 PVD sputter sources plus 1 plasma source

Want to know more?

To learn more about upcoming solutions on CLUSTERLINE® 200 for power, front or backside applications contact your local Evatec office.
https://evatecnet.com/about-us/contact-us/

Not familiar with the CLUSTERLINE® platform? Then why not watch the short CLUSTERLINE® family video to learn about Evatec's range of solutions for 200, 300 and 600mm.

Power ICs: New Cu Frontside processes on 300mm

PVD Manager Technology Development ***Mohamed Elghazzali*** tells us why Evatec's CLUSTERLINE® 300 is the ideal platform to satisfy the growing demand for 300mm processing and how Evatec process know-how is delivering high performance thick copper layers.

Why copper technology

Silicon-based devices need to improve to stay competitive from a cost and performance perspective. To achieve this, silicon power device production is moving from 200mm to 300mm wafer size and aluminum contact technology is being substituted by copper. In comparison to aluminum, copper provides higher electrical conductivity which results in lower losses and a lower Rds-on (Drain – source on-resistance). Most importantly copper is the technology of choice for Si CMOS today: A power device in copper is compatible with the front end of line processes, enabling direct integration in complex IC packages, e.g. BCD, Power IC.

Aluminum based devices are assembled by solder contact, limiting the flexibility for integration. Complex devices with higher integration require advanced packaging solutions, e.g. flip chip bumping. Advanced packaging solutions based on copper technology are the enabling solution for higher integration density (system in package, embedded dies etc.) and increased energy efficiency.

CLUSTERLINE® 300 – A platform built for front side processes

CLUSTERLINE® 300 is designed for the contamination-free processes and the low particle levels required for front side processes on 300mm. For typical Tungsten-Titanium-Alloy and thick copper single layer processes customers can expect WiW thickness / resistivity uniformities (max,min) <5% (1 Sigma <2.5%) across a 300mm wafer with edge exclusion of 3mm.

CLUSTERLINE® 300 can be configured with up to 6 process modules for degas, deposition or etch. Up to 3 load ports / FOUPS deliver wafers to the Atmospheric Frontend Module (AFEM) equipped with robot and aligner with additional options for integration of wafer buffer stations and additional Interface modules (e.g. high pressure cool). Evatec's highly efficient atmospheric batch degas (ABD) technology developed for the highest throughput Fanout and WLCSP processes is also just one of the additional capabilities that can be added for custom applications.

PVD Technology for WTi/Ti-Cu Processes

Evatec's proprietary PVD module technology is at the heart of the tool. The module enables flexibility in process geometry with target substrate distances in the range of 50 to 80mm. Hardware features focused on maintaining stable process pressures and uniform gas distribution combined with low arcing deliver the process stability and repeatabilities required for high volume production. The limited thermal budget of the substrates necessitates strict control of temperature throughout the entire 5 to 10 µm film deposition process. The principal characteristics of the recently developed cold ESC system ensure that the temperature of the wafer remains below 150°C. This has the beneficial effect of reducing the wafer bow to below 350 µm at a film stress of approximately 180 MPa. In conjunction with the specially designed cathode, this results in the ability to manage high power processes, enhancing overall productivity and providing a reliable processes with minimal in-film particle performance.

Film parameter	Performance
Thickness	5... 10µm
Deposition rate	>25 nm/s
WiW thickness uniformity	<5% (Max/min)
WiW RS uniformity	<5% (Max/min) (@ 500nm thickness)
WtW thickness uniformity	<2% (Max/min)
WtW RS uniformity	<2% (Max/min) (@ 500nm thickness)
Specific resistivity	2 ±0.3 uOhms*cm
Average film stress	app. 180 MPa
Max. wafer bow @5µm @10µm	app. 280µm app. 560µm
Max. wafer temp @5µm @10µm	<100ºC <130ºC
Mech. particles >0.16µm	< 10 adders
In-film particles >0.20µm	< 30 adders

Figure 1: Typical WTi process performance data

"Enjoy lower losses and drain source resistance with copper technology"

Lets take a look at the results

Evatec process know-how optimizes the overall process. Cathode and new developed Cold ESC chuck technologies are designed to enable maximum deposition rates for the highest throughput whilst still maintaining low substrate temperatures. Deposition conditions for both barrier and copper layers are tailored to manage overall film stack stress.

- **WTi deposition**
  Film performance data of typical WTi films in the range 50 to 200nm deposited using Evatec's PVD cathode technology is shown in Figure 1. Processes can be wide ranged tailored for either compressive or tensile film stress according to customer preference.
- **Thick Copper Layer Deposition**
  Layer performance for copper films typically in the range 5 to 10 microns is illustrated below in Figure 2. Films typically display low levels of tensile stress.

Particles and process repeatability performance

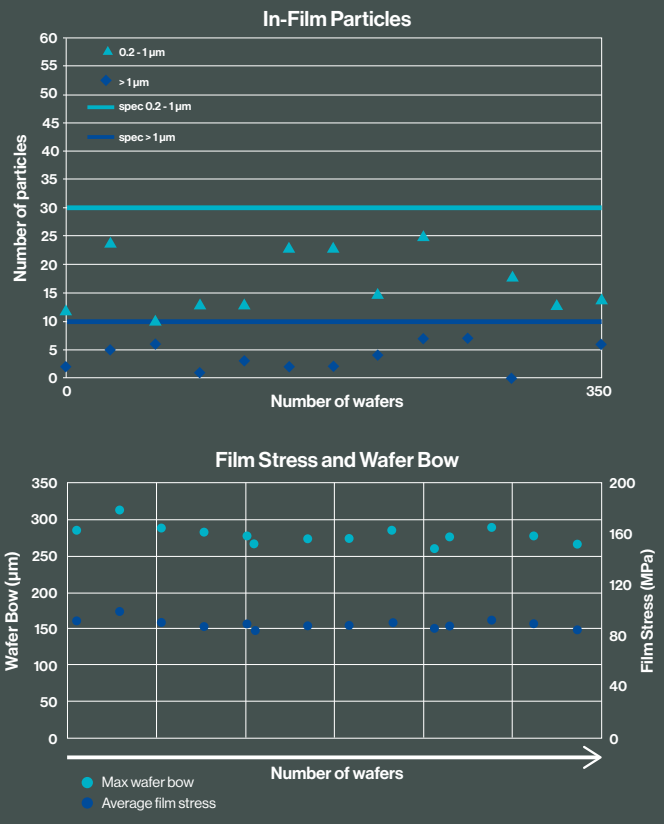


Figure 2: Thick copper deposition process stability

Low-field transport properties and scattering mechanisms of degenerate n-GaN by sputtering from a liquid Ga-target

Dr. Philipp Doering, from Fraunhofer Institute for Applied Solid State Physics (IAF) & ***Thomas Tschirky***, Evatec Senior Scientist talk about the work being done on sputtering from a liquid Ga-target.

Abstract

In this work, degenerate n-type GaN thin films prepared by co-sputtering from a liquid Ga-target were demonstrated and their low field scattering mechanisms described. Extremely high donor concentrations above 3×10^{20} cm^{-3} at low process temperatures (< 800 °C) with specific resistivities below 0.5 mΩcm were achieved. The degenerate nature of the sputtered films was verified via temperature-dependent Hall-measurements (300-550 K) revealing negligible change in electron mobility and donor concentration. Scattering at ionized impurities was determined to be the major limiting factor with a minor contribution of polar optical-phonon scattering at high temperatures. Scattering at dislocations or grain boundaries was ruled out to impact the measured mobility. The results demonstrate the huge potential of sputtering as an alternative route for the realization of low-temperature, high throughput and large-scale, regrown n-type GaN.

The use of GaN-based low-noise and high-power amplifiers as well as their advanced hetero-integration into conventional Si-CMOS technology are of major interest for next generation wireless communication systems. To meet the increased data rate requirements, higher frequencies with improved efficiency and bandwidth are targeted. However, further downscaling of the gate-length (L_G) to address higher cutoff frequencies requires significant reduction of parasitic resistances in the devices.

The access resistance of highly-scaled high-electron mobility transistors (HEMTs) or multi-channel devices suffer from the inherent metal-semiconductor barrier for high Al-content barriers. A current transport mechanism completely determined by tunneling is desirable to achieve the lowest possible voltage drop at the metal-semiconductor interface. Removing the AlGaN-barrier and/or rendering the sub-contact area n-type is the only possibility to change the electron transport across the barrier to the 2-dimension

View of the liquid Ga target through the wafer holder in the prototype sputter module

Sample	Substrate	$t_{n\text{-}GaN}$	T_H	GR	rms	FWHM (00.2)
A	GaN/Sapphire	150 nm	700°C	0.9 nm/s	0.58 nm	0.188°
B	GaN/Sapphire	150 nm	590°C	0.9 nm/s	0.38 nm	–
C	GaN/Sapphire	150 nm	800°C	0.9 nm/s	0.91 nm	0.134°
D	Sapphire	1050 nm	800°C	0.6 nm/s	21.6 nm	0.437°

Table 1: Structural properties of co-sputtered n-GaN: $t_{n\text{-}GaN}$ – thickness of Si-doped GaN-layer, T_H – nom. Heater temperature, GR – growth rate, rms – root mean square, FWHM - full-width half maximum of the 00.2.

electron gas (2DEG) from a thermionic to field-emission type at higher Al-contents. However, to achieve the high doping concentrations ($N_D > 1\times10^{20}$ cm^{-3}) for a completely field emission based current transport is difficult due to the decreasing crystal quality. In addition, low temperature processes on a large wafer scale are beneficial to protect the AlGaN/GaN-interface in a HEMT or for a direct III-Nitride hetero-integration of (opto-)electronic devices on a Si-based platform.

In this work, the transport properties of heavily Si-doped GaN thin films deposited by co-sputtering from Si and a liquid Ga-target and on 4-inch sapphire substrates are investigated. Extremely high effective donor concentration ($N_D > 3\times10^{20}$ cm^{-3}) are demonstrated. Specific resistivity below 0.5 and 3.5 mΩcm are achieved at growth temperatures of 800°C and 590°C, respectively. Carrier mobilities were found to be limited by scattering at ionized impurities at the high Si doping levels. Donor-acceptor compensation ratio was found nearly constant below $\theta \approx 0.2$ even beyond $N_D > 1\times10^{20}$ cm^{-3} different to reported data by metalorganic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE). Temperature-dependent Hall-measurements revealed negligible change in carrier density and mobility with increasing temperature indicating Mott-transition from a semiconducting to a metallic character. Carrier densities and specific resistivity at low growth temperatures (≤ 800 °C) are found well beyond reported data of MOCVD-grown thin films. The results demonstrate the feasibility of sputtered GaN from a liquid Ga-target as alternative process with high carrier density and easy upscaling beyond 4-inch suitable for future process integration into future radio-frequency or optoelectronic (e.g., tunnel junctions) GaN-based devices.

Recent focus on the development of advanced contact processes is generally driven by CMOS-compatible, Au-free and/or low temperature budget ohmic contacts, or n-GaN regrowth for highly-scaled AlGaN or novel Al(Sc)N-based HEMTs with high Al-content. The fabrication of highly n-type doped GaN films was demonstrated via Si-implantation, MBE, MOCVD (Si or Ge), pulsed laser deposition (PLD) and reactive, pulsed sputtering (PVD) from a solid Ga-target (Si, Ge, Sn, O). Si-implantation is used for GaN-devices but faces issues to achieve carrier densities above 1×10^{19} cm^{-3} and requires a high-temperature treatment to recover for the implantation damage. MBE-regrown ohmic contact layers are currently the method of choice due to the low growth temperature but faces issue in terms of upscaling, throughput and homogenitiy. MOCVD regrowth was demonstrated via flow-modulation epitaxy at low growth temperatures with reduced growth rate, but faces limitations in terms of achievable carrier density beyond $5\text{x}10^{19}$ cm^{-2} at 550 °C and does not offer a non-selective growth mode to avoid growth rate inhomogeneities. Typical growth temperatures with high growth rates are conducted at much higher temperatures (> 950 °C). Reactive sputtering was demonstrated with high carrier density and high mobility on 300 – 600 nm thick films. However, the used solid Ga-targets need to be heavily cooled to remain solid during sputtering. In addition, the cooling system gets more complex for larger wafer diameters and impurity concentration in e.g., ceramic Ga is not easy to handle. The use of a liquid Ga-target avoids the need of a complex cooling-system required to keep solid Ga-targets below its melting point. The liquid target can be easily filled up and no sputter craters occur during growth. In addition, the liquid target can be easily upscaled to larger wafer diameters (> 2-inch) as well as lower unintentional/parasitic doping occurs when compared to a ceramic Ga-target.

4-inch sapphire substrates were used for the deposition of the conductive thin films. Three samples (A-C) were initially grown by metal-organic chemical vapor deposition with an Fe-doped buffer to render the GaN-layers semi-insulating topped with a 200 nm unintentionally-doped GaN layer to compensate for Fe-segregation. The sheet resistance of samples A, B and C were measured after MOCVD buffer growth via contactless Eddy-current revealing a $R_S > 100$ kΩ/sq, which is the upper measurement limit of the setup. GaN films were deposited by co-sputtering of a Si-bar and a liquid Ga-target in an Evatec CLUSTERLINE® 200II with a modified process module. 150 nm Si-doped GaN were sputtered on top of the MOCVD-GaN with nominal growth temperature of 590, 700 and 800 °C. Sample D was prepared by directly sputtering GaN:Si on Sapphire. Rocking curves of the 00.2-reflex were carried out by X-ray diffraction to determine the full-width half maxima (FWHM). FWHM were derived from fitting of two pseudo-Voigt functions assuming that the peak with lower intensity is related to the sputtered, Si-doped GaN. The FWHM of the MOCVD-grown buffer was found to be FWHM = 0.064°. Fitting of the sample with lowest growth temperature was not possible due to the low intensity of the second peak. However, it can be concluded that lowering the heater temperature leads to a slight decrease in crystal quality.

Atomic force microscopy (AFM) was used to determine the root mean square (rms) to revealing smoothest surface morphology with lowest growth temperature. A summary of the structural properties is given in Table 1.

Originally published with references in Applied Physics Express 17(3), 031003 (2024) (https://doi.org/10.35848/1882-0786/ad3367)

The theoretical metal-semiconductor transport properties (thermionic emission - TE, thermionic field emission - TFE; field emission – FE) are dependent on the characteristic energy E_{00}, which in turn is dependent on the carrier density in the sub-contact area as following:

$$E_{00} = \frac{qh}{4\pi}\sqrt{\frac{N_D}{\varepsilon_r\left(\frac{m_{tun}^*}{m}\right)}}$$

With q, h, ε_r (9.5), m_{tun}^* and m ($m_{tun}^*/m = 0.22$) are the elementary charge, Plancks constant, relative dielectric constant, effective tunneling mass, and electron mass, respectively. We use the simple differentiation: FE: $E_{00} \leq 0.5$ kT; TFE: 0.5 kT $\leq E_{00} \leq 5$ kT and $E_{00} \geq 5$ kT. Thus, to achieve $E_{00} \geq 5$ kT a donor concentration of $N_D > 1\times10^{20}$ cm^{-3} is required for GaN. Fundamental low-field transport properties are characterized by Hall-measurements at room-temperature (RT). Ti-based ohmic contacts were evaporated via shadow masks and 4-terminal structures mechanically isolated. The use of a co-sputtering of a Si-bar comes along with the possibility to achieve a gradient in Si-concentration over the same wafer depending on the distance of the wafer area to the Si-bar. Thus, several carrier concentrations and corresponding carrier mobilities can be measured on the same wafer. Carrier densities of $N_D = 6.7\times10^{19}$ to 3.7×10^{20} cm^{-3} with carrier mobilities of $\mu = 21$ to 42 cm²/Vs were found over all samples. Improved compensation ratios were found with increasing heater temperature as given in Figure 1. The achieved carrier densities are well beyond the state of the art reported for MOCVD ($N_D < 2.2\times10^{20}$ cm^{-3}) and MBE ($N_D < 2\times10^{20}$ cm^{-3}) at generally lower growth temperature (Figure 1c). The achieved carrier densities are exceeding the the $E_{00} \geq 5$ kT = $N_D >$ 1×10^{20} cm^{-3} requirement described before. In addition, the extremely high carrier concentrations would be well suited e.g., to address source starvation issues causing linearity distortion in highly scaled GaN-HEMTs.

In general, several scattering mechanisms could be assumed for the co-sputtered GaN:Si even though impurity scattering is most likely dominating at high donor concentrations. Scattering at ionized impurities in dependence of the compensation ratio $\Theta = N_D/N_A$ can be expressed by:

$$\mu_{II} = 3(\varepsilon_0\varepsilon_r)^2\left(\frac{h}{q}\right)^3\left(\frac{n}{N_I}\right)\left(\frac{1}{m^*_F}\right)\left(ln(1+\beta_F{}^2) - \frac{\beta_F{}^2}{1+\beta_F{}^2}\right)^{-1}$$

With:

$$\beta_F{}^2 = \frac{16m^*_e\varepsilon_0\varepsilon_r E^2_F}{3q^2h^2n}$$

And N_I and m^*_F are the ionized impurity concentration and effective mass at the Fermi energy, which is given by:

$$m^*_F = m^*_e\left(1+\frac{6\alpha E_F}{E_g}\right)$$

with

$$E_F = E^0_F\left(1+\frac{\alpha E^0_F}{E_G}\right)$$

and:

$$E^0_F = \left(\frac{h^2(3\pi^2 n)^{2/3}}{2m^*_e}\right)$$

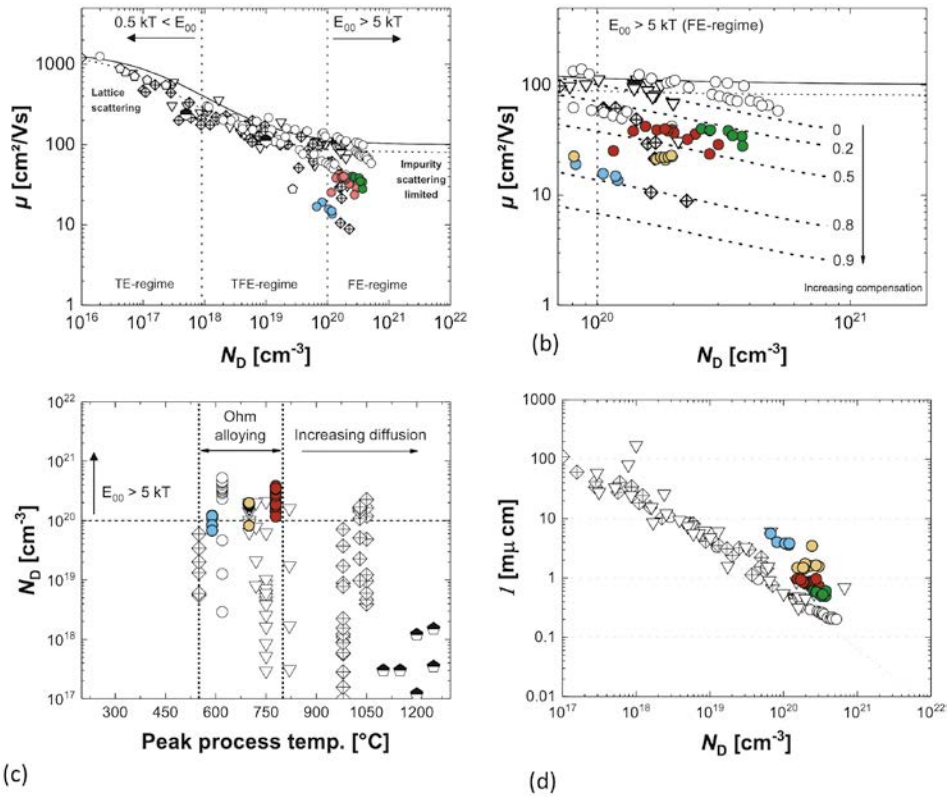


Figure 1: (a) Donor concentration vs. carrier mobility reported in literature for various growth methods: metalorganic chemical vapor deposition (quarters with cross); molecular beam epitaxy (diamonds); hydride vapor phase epitaxy (pentagons) reactive sputtering (grey circles); Si-implantation (half-filled hexagons). Samples in this work are colored: sample A (yellow); B (blue); C (red); D (green). Solid and dotted lines represent fitting from Schwierz et al. based Caughey-Thomas approximation; (b) N_D vs. μ in the range of $E_{00} > 5$ kT. (c) Peak process temperature vs. measured donor concentration. Reported range of alloying temperatures of ohmic contacts to AlGaN/GaN are added as a reference; (d) carrier concentration vs. specific resistivity.

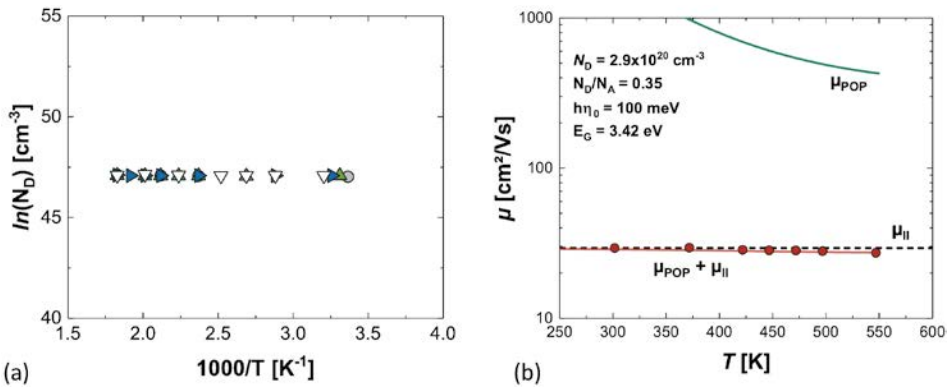


Figure 2: (a) Arrhenius plot of three different positions of sample C; (b) Temperature dependent electron mobility of the heavily doped GaN. Scattering by ionized impurities μ_{II} (black)b and polar optical-phonons μ (green) was modelled to fit the experimental data (red).

Where α (0.64) and m^*_e (0.22m_e) are the non-parabolic conduction band coefficient ($\alpha = 1(m^*_e/m_e))^2$, and the electron effective mass, respectively. High carrier compensation ratios $\theta = N_D/N_A$ were found for MOCVD and MBE grown samples beyond $N_D > 1\times10^{20}$ cm^{-3} as shown in Figure 1b. In consequence, strong mobility decrease was reported limiting the achievable carrier density and specific resistivity. Compensation ratios of the co-sputtered thin films in this work were found to be rather constant up to $N_D = 3.7\times10^{20}$ cm^{-3} at higher growth temperatures. A significant increase in compensation ratio (is observed at lower growth temperatures ($\theta = 0.8$), which could be attributed to a decrease in crystal quality where e.g., increasing amount of point defects (e.g., Ga-vacancies). The assumption is consistent with the increase in FWHM and decrease in peak intensity of the second 00.2-reflex observed by XRD. Only reactively sputtered thin films on 2-inch substrates from solid Ga-targets were reported with even higher carrier mobilities in the same range of carrier densities so far. Reported data are even higher than the impurity scattering limit at $\theta = 0$, which was stated to be the result of an underestimation of the effective electron mass but not further discussed. Specific resistivity was derived and compared to reported data from the literature (Figure 2). Lowest specific resistivities in this work were obtained for highest growth temperature (800°C) with $\rho < 0.5$ mΩcm which is close to best reported values in literature independent of the growth method. An increase of resistivity is observed by lowering the growth temperature as a result of the increasing compensation ratio described before. Lowest resistivity of sample A (590°C) was found to be 3.5 mΩcm. The measured carrier concentrations are well beyond the theoretically, required doping to achieve a metallic character. To verify Mott-transition of the sputtered GaN films, temperature-dependent Hall measurements were carried out for T = 300 to 575 K. No significant change in electron concentration or electron mobility was observed within the measured temperature range indicating the degenerate nature of the Si-doped GaN films. Temperature-dependent polar optical-phonon scattering was modelled via:

$$\mu_{POP} = \frac{\varepsilon_0 \varepsilon_r \hbar}{eNm^*_F} \sqrt{\frac{\hbar}{2m^*_F \omega_0 (1 + \hbar\omega_0/E_G)}} \left(1 - 5\frac{k_B T}{E_G}\right)$$

where $\hbar\omega_0$ is the optical phonon energy (100 meV). Scattering at dislocations is neglected since their impact on transverse mobility above $N_D > 1\times10^{20}$ cm^{-3} for dislocation densities below $N_{DISL} < 1\times10^{11}$ cm^{-2} is not relevant. Dislocation densities of MOCVD-grown GaN on sapphire with AlN nucleation layer (templates used in this work) are generally found to be lower much lower and the interface of sputtered GaN on MOCVD-GaN is not expected to generate new dislocations. Scattering at grain boundaries could be assumed for sputtered GaN, however, the associated potential barriers would lead to a thermal activation of the carrier mobility or carrier density. In addition, at high doping levels, most of the grain boundary related trap states are filled and the potential barriers would decrease in height and width. Temperature dependent fitting of the carrier mobility was achieved using Equation 2 and 7 by Matthiessens rule given in Figure 2b. Only minor contribution of μ_{POP} was found while μ_{II} clearly dominates the overall low-field scattering in the samples.

In conclusion, heavily doped GaN thin films prepared by co-sputtering from a liquid GaN-target were demonstrated. Extremely high donor concentrations above 3×10^{20} cm^{-3} at low process temperatures (< 800 °C) with specific resistivities below 0.5 mΩcm were achieved. Mott-transition was verified via temperature-dependent Hall-measurements revealing neither a change in mobility nor carrier concentration in the range of 300 to 550 K. Impurity scattering was determined to be the major low-field mobility limiting factor with a minor contribution of polar optical-phonon scattering at elevated temperatures. Scattering at dislocations or grain boundaries was ruled out to impact the total mobility. The results demonstrate the huge potential of sputtering as an alternative route for low-temperature, high throughout and easy upscaling of regrown n-type GaN.

A freshly filled Ga target bowl. Inset: Process of filling liquid Ga

HEXAGON
Throwing a double in power device applications

Evatec's CLUSTERLINE® family of 200 and 300mm have a worldwide reputation as flexible, secure production solutions across a wide range of front and backside processes in power applications. But we like to stay ahead of the game especially when it comes to driving down cost of ownership. Read on as Product Marketing Manager, ***Fabian Kramer*** & Senior Process Engineer, ***Gerald Feistritzer*** give us an idea how HEXAGON could double your throughput in selected power device applications.

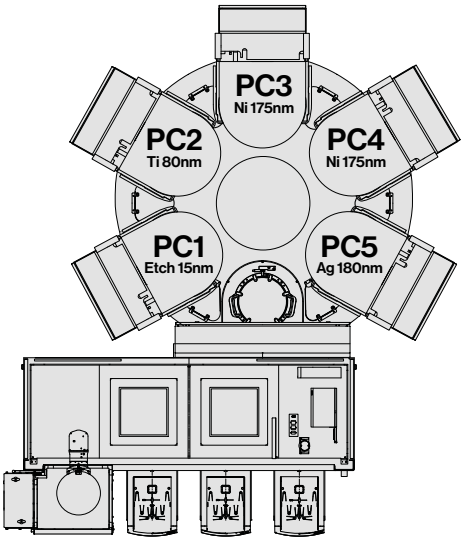
The challenge

Backside metallization has always been a sensitive market when it comes to cost of ownership. Evatec has been delivering solutions on silicon using CLUSTERLINE® for many years where secure thin wafer handling and management of stress are vital for the best process reliability and wafer yields. The market for applications using wide band gap (WBG) materials is also now developing strongly, so it's time to look at how we can help our customers develop the best production solutions for devices based on these new materials.

The new generation HEXAGON is already also known by many of our customers for delivering industry leading throughput and process performance in Advanced Packaging applications like FOWLP. Its "inline" configuration offering high speed wafer transfer and fast pumping offers a new approach for increasing throughput and driving down cost of ownership in selected power applications too, so lets take a look at some typical examples for processes for bonded or unbonded SiC wafers.

Case study 1: Thin SiC wafer – direct handling without carrier

Tool configuration

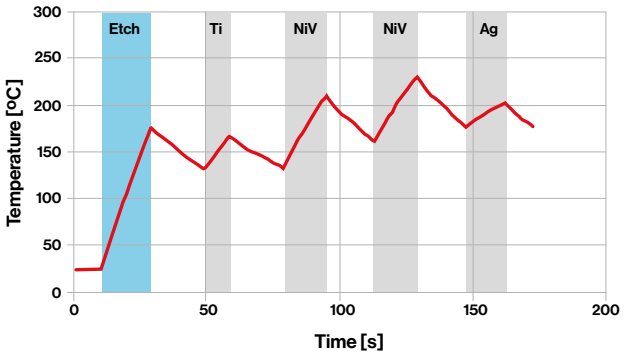


Results

Throughputs of up to 80 wafer per hour could be achieved. This is thanks to the short transfer times, rapid pump down, gas stabilization and pump clean steps inherent in HEXAGON architecture. Processing temperatures are also within the normal range compared with conventional processing on CLUSTERLINE®.

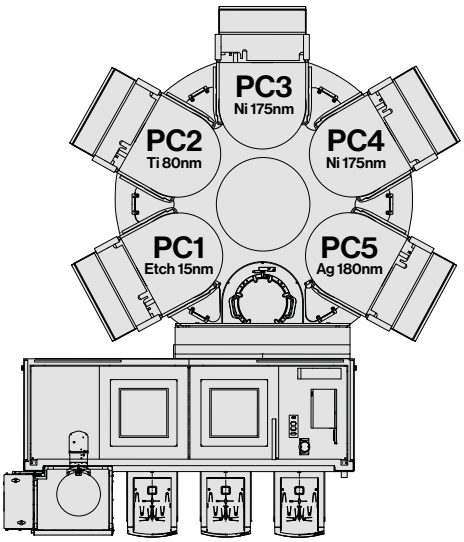
Assumptions

- Etch 15nm / Ti 80nm / NiV 350nm / Ag 180nm
- Thin SiC 250µm
- No T-limit



Case study 2: Thin SiC wafer bonded on glass carrier

Tool configuration

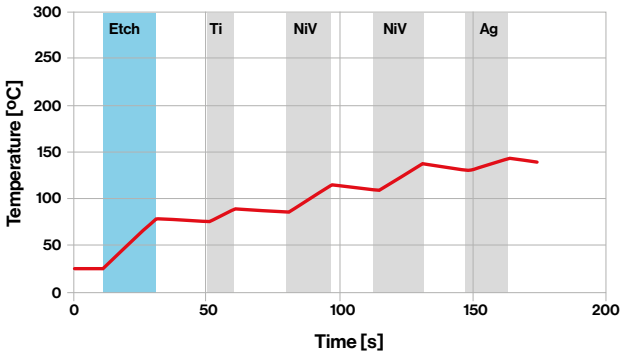


Results

Just like the first case study, the short transfer, pump down, stabilization and pump clean times give HEXAGON an immediate advantage but still enable process temperature to be controlled within the restricted range allowed for bonded wafers of 150°C in this specific case. Throughputs >75 wafer per hour were achieved.

Assumptions:

- Etch 15nm / Ti 80nm / NiV 350nm / Ag 180nm
- Thin SiC 100µm bonded on glass carrier 900µm
- 150°C T-limit



HEXAGON – the solution for everything?

Of course not! CLUSTERLINE® along with its configuration for up to 6 cathodes, complete range of chuck options including clamping and reputation for the ultimate in temperature and therefore bow control still provides the most flexible solution in the market, but if HEXAGON can fulfill your process specs its undoubtedly a winning throw of the dice.

Find out if HEXAGON is the right tool for you

Our process team would love to talk to you and explore if HEXAGON could be the perfect fit for your application. Scan the QR code now to contact us to take the first step.

COMPOUND & PHOTONICS NEWS

CELEBRATING 20 YEARS OF DEVELOPMENT AT EVATEC

Slowly but surely, Quantum Computing will transform industry and society

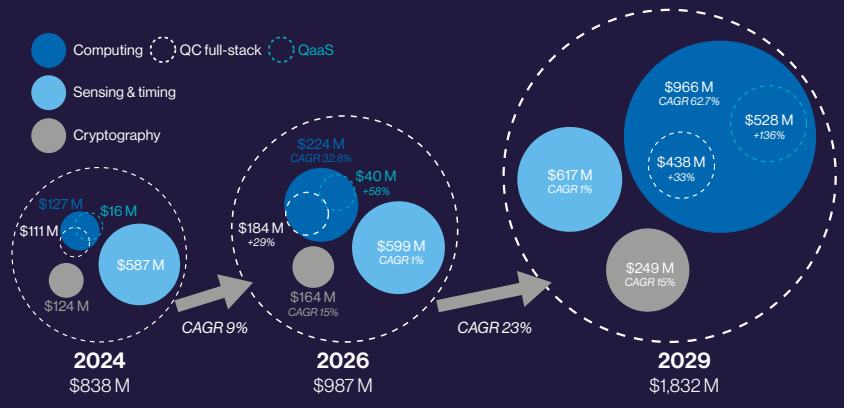
Dr. Eric Mounier of Yole Group talks about both the market potential and supply chain challenges to be overcome to see the successful launch of Quantum Computing Services in the next decade.

In recent years, there has been significant excitement surrounding quantum technologies. Quantum effects can be harnessed for various applications, including ultra-sensitive sensors like gravimeters and atomic clocks, and ultra-secure communication (cryptography). However, the application that garners the most attention and funding, both from private and public sources, is quantum computing. The primary advantage of quantum computers lies in parallelization, enabling simultaneous calculations that offer substantial time and energy savings, along with enhanced computing power.

The potential applications of quantum computing span various sectors, including finance (for anticipating financial risks), healthcare (reducing the time and cost of discovering new drugs, which currently takes 10+ years and billions of dollars), optimizing materials for electric vehicle batteries, and, of course, defense. Consequently, quantum computing has become a strategic priority for countries worldwide, leading to significant investments in research and innovation. Global investments in quantum science and technology currently approach $30 billion, with notable contributions from the USA, China, and Europe (about $5 billion each).

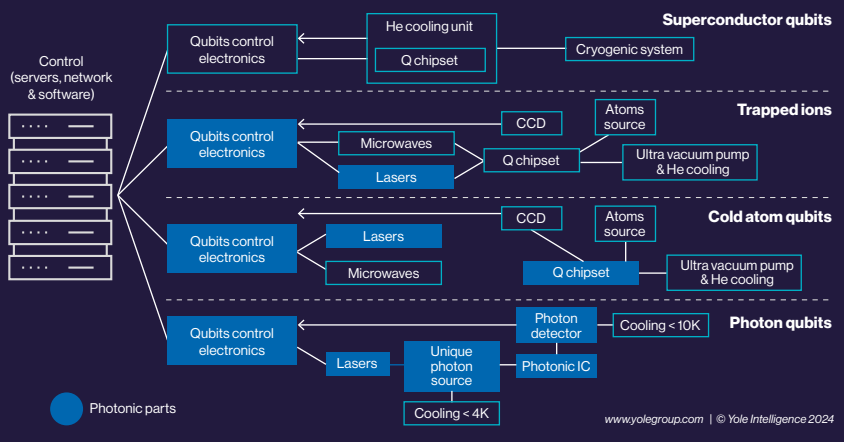
2024-2026-2029 Quantum Technologies Forecast

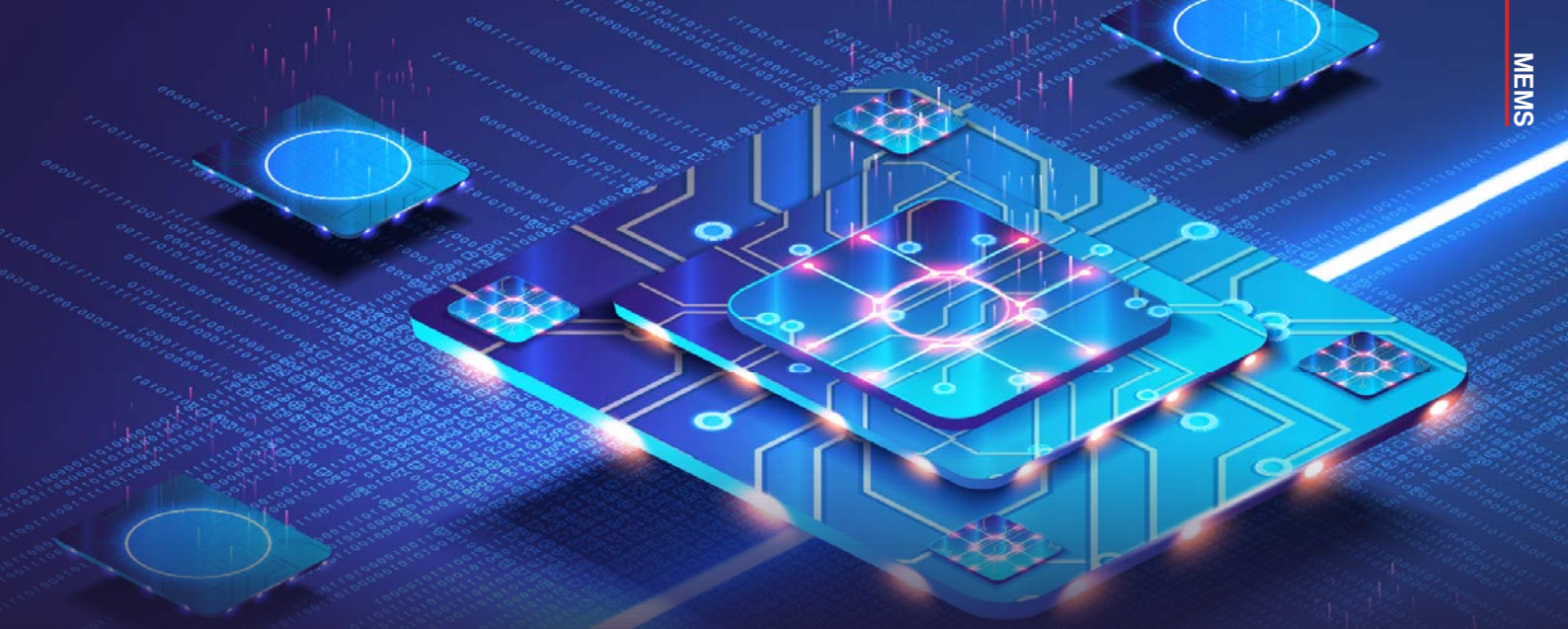
Source: Quantum Technologies report, Yole Intelligence, 2024



The different architectures of Quantum Computers

Source: Quantum Technologies report, Yole Intelligence, 2024





On the supply chain side, the quantum ecosystem is maturing and strengthening through collaborative research projects, the development of patent portfolios, the establishment of startups, and the involvement of semiconductor vendors and equipment makers such as Intel, TSMC, GlobalFoundries, Xfab, and SkyWater. Today, a handful of companies, including D-Wave, IonQ, Rigetti, PsiQuantum, and Xanadu, dominate nearly 70% of global funding in this domain. Each year sees the emergence of numerous quantum startups, primarily in computing, and a complete supply chain is being set up at each level: software, materials, tools, devices, systems, and end-users.

However, the path to achieving quantum supremacy is fraught with challenges. In the quantum world, the equivalent of a bit is a qubit, which can exist in a superposition of both 0 and 1. Qubits are, unfortunately, highly sensitive to errors induced by external factors such as temperature and radiation, necessitating operation in ultra-cold environments. Consequently, quantum computers are highly complex systems with a current price tag of about $15 million. We do not foresee a dramatic cost reduction in the short term.

While practical use cases for quantum computing are still far from being realized, technological developments are progressing well despite the continuous race to achieve the largest number of qubits. We estimate that by 2030, a few dozen quantum computers will be operational worldwide for private use (finance and defense industries are quite eager to have their own quantum computers on-premises for security reasons) and installed at quantum manufacturers' sites that will rent quantum calculation time (QaaS or "Quantum as a Service" business model).

Optimism about the success of quantum technology persists, fueled by significant technological advancements and investments worldwide. Quantum computing hardware is projected to grow from $111 million in 2024 to $438 million in 2029 (26% CAGR). QaaS will increase from $16 million in 2024 to $528 million in 2029 (85% CAGR). Beyond 2030, we forecast the quantum computing market will total $3.74 billion in 2035 (both hardware and service). QaaS (Quantum as a Service) will constitute the major share of this value, with most services running on quantum computers in the cloud. It will grow much faster than quantum computer hardware as we expect to see more use cases being developed for quantum computers before 2030.

About the author

Eric Mounier, Ph.D., is Chief Analyst, Photonics & Sensing at Yole Group.

With more than 30 years' experience within the semiconductor industry, Eric provides daily in-depth insights into emerging semiconductor technologies such as quantum technologies, the Metaverse, terahertz, photonics, and sensing.

Based on relevant methodological expertise and a significant technological background, Eric works closely with all of Yole Group's teams to highlight disruptive technologies and analyze business opportunities through technology & market reports and custom consulting projects.

Eric has spoken at numerous international conferences, presenting Yole Group's vision of emerging semiconductor technologies, markets, and applications. Previously, Eric held R&D and Marketing positions at CEA-Leti (France).

Eric Mounier has a Ph.D. in Semiconductor Engineering and a degree in Optoelectronics from the National Polytechnic Institute of Grenoble (France).

BAW technology – AlScN based RF filters

Helping customers keep the lead in 5G and beyond

Evatec Product Marketing Manager for Wireless applications ***Dr. Oguz Yildirim*** shows how the latest thin film processes for deposition of both piezoelectric layers and electrodes are helping customers keep leading performance in BAW filter technology.

CLUSTERLINE® 200 – The market leader in BAW

Evatec is already well established in delivering thin film production solutions for BAW technology. Previous edition of *LAYERS (LAYERS 6, page 60)* have already reported on the work developing production tools and processes for deposition of high Sc content Piezoelectric films of up to 30%. Today there are more than 150 Evatec modules working in 24/7 production around the world at uptimes higher than 95%. CLUSTERLINE® 200 which can be equipped with up to 6 single process modules and front end cassette or SMIF ports and ARQ 151 cathode technology utilizing 304mm diameter targets is the workhorse to deliver the excellent WiW thickness and stress uniformities demanded by our customers. Now however, our new generation ARQ320 cathode provides even better uniformities and longer lifetimes, improving the cost of ownership (CoO) by one more step.

Bulk acoustic wave (BAW) filters used in RF front end modules enables high speed, large bandwidth data transfer rates in our mobile phones paving the way for 6G, next generation communication (see Figure 1). BAW devices are based on a piezoelectric thin film excited via bottom and top electrodes that are in contact with the piezoelectric layers.

Figure 1: Bulk acoustic wave (BAW) filters.

8 out of 10 mobile devices on the market equipped with BAW RF filters contain Evatec layers

Piezoelectric layers

Taking AlScN performance to the next level by moving to Sc content >30at %

The ongoing move towards transferring larger amounts of data at even higher operating frequencies calls for higher scandium content and thinner films but this must be achieved without compromize on film quality. Average stress and its variance across the wafer must remain under control and film surface quality must be kept free of abnormally oriented grains typically seen at higher Scandium levels. And all this without any compromize on very low levels of edge exclusion on the wafer to maintain manufacturing process yield. Figure 2a shows the gains in piezoelectric coefficient possible by moving to higher scandium content, while Figure 2b shows the variation in electromechanical coupling coefficient as a function of film stress as reported in the literature. This reminds us of the importance of achieving excellent thickness uniformity and narrow stress range across wafers in production.

Typical process performance on 200mm in production is illustrated in Table 1, allowing customers to achieve the highest wafer utilizations with edge exclusion of only 5mm.

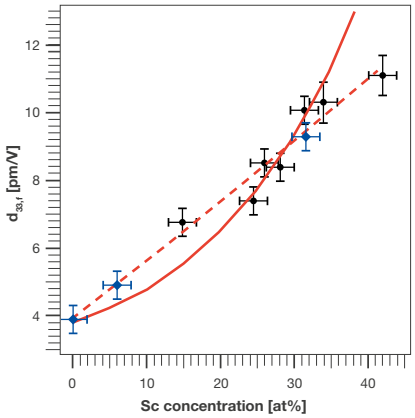


Figure 2a: $d_{33,f}$ as a function of the Sc content. Solid red curve represents the value obtained from ab-initio calculation

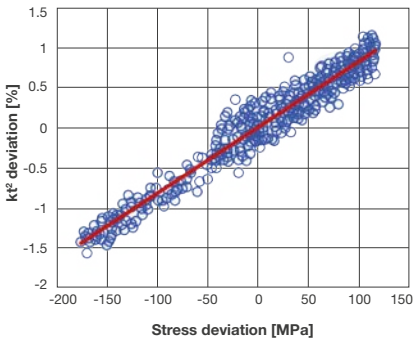


Figure 2b: Coupling coefficient vs stress for $Al_{0.7}Sc_{0.3}N$ film

$Al_{1-x}Sc_xN$ film performance on 200mm

Substrate	Film Parameter
Wafer diameter	200 mm
In film Sc concentration	Up to 39 at.%
Film thickness	500nm
Thickness uniformity (within wafer) 1sigma	<0.5%
Thickness uniformity (wafer to wafer) 1sigma	<0.3%
Refractive index @633nm wavelength	2.07
Average film stress range	-300 to +500 MPa (adjustable)
Film stress range (within wafer)	±75 MPA(@0.5% Uth) ±50 MPa (@ 1.0%Uth)
Stress repeatability (wafer to wafer)	±30 MPa
Rc <002>	< 1.5° (FWHM)

Table 1: Typical process performance

Surface quality of high scandium content films

Figure 3 shows the results by AFM obtained from $Al_{1-x}Sc_xN$ layers where x is varied from 20 at.% to levels higher than 36 at.% in the target material resulting in $Al_{1-x}Sc_xN$ layers with average Sc concentrations up to 39.7 at.%. These were produced on a CLUSTERLINE® 200 using a "manufacturing ready" single target source. These layers have been qualified at a wafer and device level. Based on the results we show the deposition path towards the experimentally achievable limit of Sc doping. However, Sc atoms in the AlN lattice can also lead to defects resulting in abnormally oriented grains (AOGs) or depending on the growth conditions phase segregation. Formation of such defects is the biggest challenge for growing highly uniform, stress neutral $Al_{1-x}Sc_xN$ thin films while can already offer production ready solution for Sc concentrations up to ~40at.%.

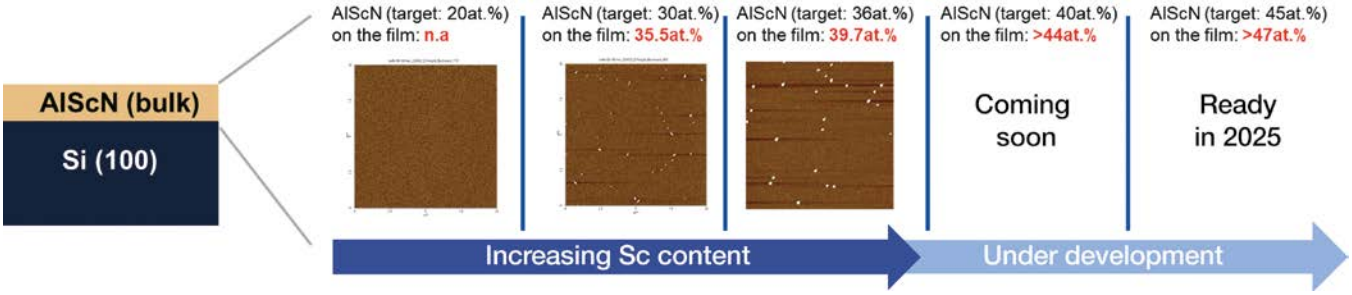


Figure 3: AFM image of $Al_{1-x}Sc_x$ N layers for varying Sc doping levels and 500nm thickness. All these layers were grown during production simulation depositions on 8 inch wafers, and have thickness uniformities <0.5 % (1 sigma), neutral average stress and stress range <150MPa. Sc concentration of the target consistently varies from the measured average Sc concentration in the film.

Electrodes

Delivering the best piezoelectric layers may rightly get lots of attention, but that's not the whole story and we can provide unique solutions for electrode production that provides flexible processes.

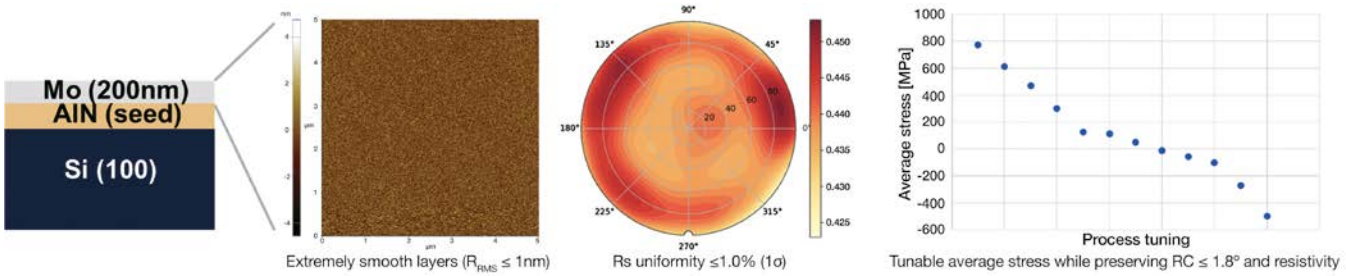


Figure 4: Performance of standard production solution of Evatec Mo layers grown on polycrystalline seed layers. From left to right are; schematic of layers, AFM image, Rs map and average stress data. Average stress is tuned while the other layer properties kept the same.

Current state of the art

Evatec's existing hot Electrostatic Chuck (ESC) technology is already well known as a standard production solution for tuneable electrode deposition processes delivering smooth, highly conductive layers and controlled stress. Our standard production solution gives the flexibility to tune the average stress of the electrode layers while maintaining the basic film performance such as the crystal quality, resistivity and uniformities. Typical results are shown in Figure 4. Further development can be done utilizing our unique sputtering based epitxial seed layer solution prior to electrode deposition. This results in a significant improvement in specific resistivity, roughness and crystal structure without increasing the deposition temperature during the growth of the Mo layer. The results are shown in Figure 5.

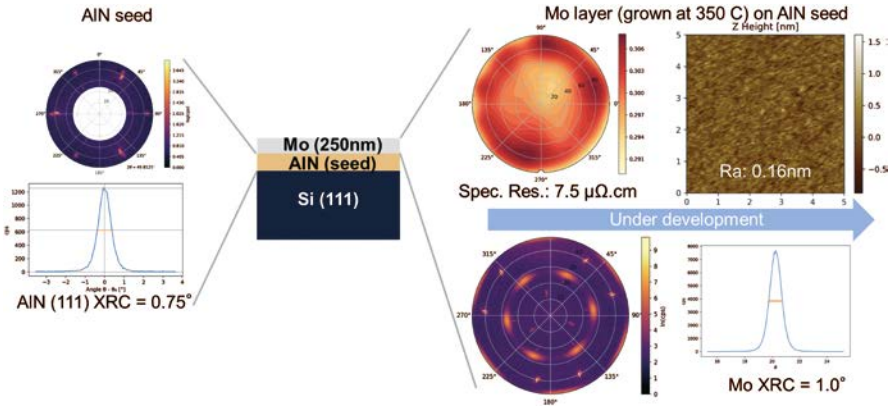


Figure 5: Properties of Epi-AlN seed layer (left) and Mo layer grown on Epi-AlN seed layer (right).

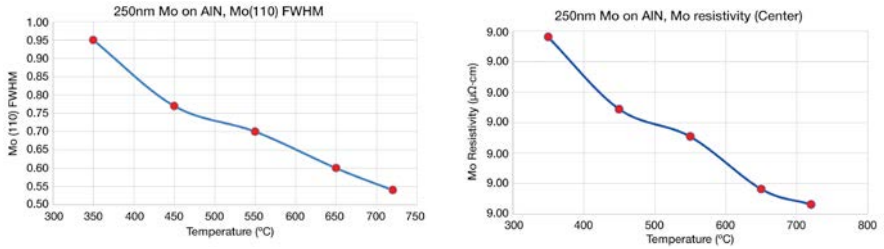


Figure 6: Properties of new generation, very hot Mo layers grown on Epi-AlN seed layers. FWHM of the Mo(110) rocking curve (left), and resistivity (right).

Electrode processes – The future is already here!

Often the electrode materials chosen for BAW applications are so-called high melting point materials comprising of elements such as W, Mo, etc. Further improvement on layers based on these materials thus require production solutions at high temperature. The most recent developments at Evatec are focused on offering customers Very Hot Chuck (VHC) capability at temperatures up to 750ºC and with it, the possibility to achieve significant reductions in resistivity and improvement in the film crystallinity that enhances the device performance dramatically as shown in Figure 6.

Multi BAK – Continuing to push boundaries in evaporation technology

It is only three years since Evatec launched the ground breaking Multi BAK concept. We took our know-how in automated handling and loadlock technology and combined it with up to 4 BAK process chambers in a clustered configuration. This brings even greater levels of process repeatability and enhanced throughput for high volume applications. Evatec Manager Customer Engineering ***Marco Stupan*** tells us about the latest Multi BAK platform capability developments giving customers across typical applications in wireless, power and optoelectronics even greater production choice.

New capabilities in substrate handling

The original platform based on Atmospheric Front End Module (AFEM) with cassette ports was launched in 2021. Since then we have added Standard Mechanical Interface (SMIF) ports as an alternative load port solution. This configuration has enabled handling of thinner wafers and is ideal for those customers looking to integrate the tool within fully automated fabs. The single process module configuration BAK911 with manual wafer loading also remains available. Table 1 compares the substate management capabilities of each configuration in the portfolio.

	BAK 941E – AFEM with Cassette Loadports	BAK 941E – AFEM with SMIF Loadports	BAK 911E – Manual Wafer Loading
Supported wafer sizes	150mm, 200mm	150mm, 200mm	Any type that fits on the calotte
Fully automatic wafer handling	✓	✓	✗
Mixed Operation of different wafer sizes (Bridge tool)	✓	✗	✓ (manual loading)
Substrate Introduction	Open cassette with vertically oriented substrates	SMIF pod or adapter pod for cassette loading	Manual loading of pre-loaded calotte segments or directly substrates
Aligner Type	In cassette batch aligner	Single wafer chuck type aligner	n/a
Warped / bowed wafers	✗	✓ (max ~3mm)	✓
Wafer Thickness	>250µm	> ~120µm	Any
Wafer ID reader	✓	✓	✗

Table 1

Material Management

To maximize throughput of these systems we need to optimize material management, extending the time between process chamber venting for refill of sources. Multi BAK can now be equipped with single or twin electron beam guns with multi pocket crucibles and wire feeders to achieve a maximum amount of process runs before it's needed to vent the chamber for refilling and cleaning.

The Multi BAK – delivering other benefits too!

To maximize throughput of these systems we need to optimize material management, extending the time between process chamber venting for refill of sources. Multi BAK can now be equipped with single or twin electron beam guns with multi pocket crucibles and wire feeders to achieve a maximum amount of process runs before it's needed to vent the chamber for refilling and cleaning.

"Multi BAK – reducing energy consumption compared with conventional stand alone platforms by up to 60%"

SPOTLIGHT ...Multi BAK

Why Multi BAK?
It is all about automation and throughput!

The driving force at the time of the platform launch in 2021 was to remove manual wafer loading by the operator and to increase the throughput. Evatec's LLTM technology essentially eliminates the pump down time out of the throughput equation.

The AFEM removes all human handling of wafers to load the calottes and provides a high class clean room environment to do so. Table 2 shows how throughput compares between a traditional system and a system equipped with LLTM based on the evaporation process times.

PROCESSING TIME (min)	CLASSIC BAK (Batch/h)	BAK WITH LLTM (Batch/h)	BENEFIT FACTOR
20	0.67	1.76	2.6
40	0.55	1.11	2.0
60	0.46	0.81	1.8
90	0.38	0.58	1.5
120	0.32	0.45	1.4
180	0.24	0.31	1.3
240	0.19	0.24	1.2

Table 2

One concept – Multiple configurations optimized for your process and throughpout

Designed for up to 4 process chambers the Multi BAK delivers:

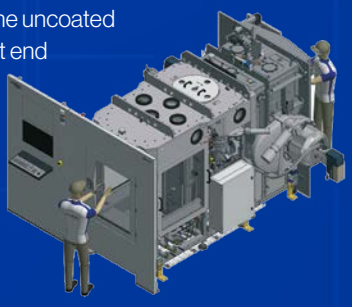
- Front end automation of wafer loading (6 or 8 inch), directly from cassettes to calotte segments in a controlled environment eliminating risk of operator errors and reducing risk of particles, wafer damage or breakage
- Automated substrate journey management to ensure a return of each substrate to the original cassette and slot.
- Wafer ID reading on the fly
- Tracking of each and every wafer to an individual location, segment or process batch

Watch the Multi BAK video

Starter configurations are available too

For single process chamber configuration the system can also be configured with manual segment loading and removal, but still with the same LLTM technology to retain the benefits of higher throughput and reduced energy consumption.

- The complete process chamber remains under vacuum continuously, delivering the most stable process environment possible for even greater levels of process repeatability when required
- The only elements entering and leaving the process chamber during production are segments loaded with wafers. They enter and leave the process chamber via a LLTM
- Rapid pump and transfer in this step offers a great opportunity to make additional overall gains in throughput
- Sources replenished by the wire feeder remain under vacuum in a ready state for the highest stability. Opening of the process chamber itself is then limited to periodic maintenance such as pocket cleaning and shield change
- An operator loads and unloads the uncoated and coated segments at the front end

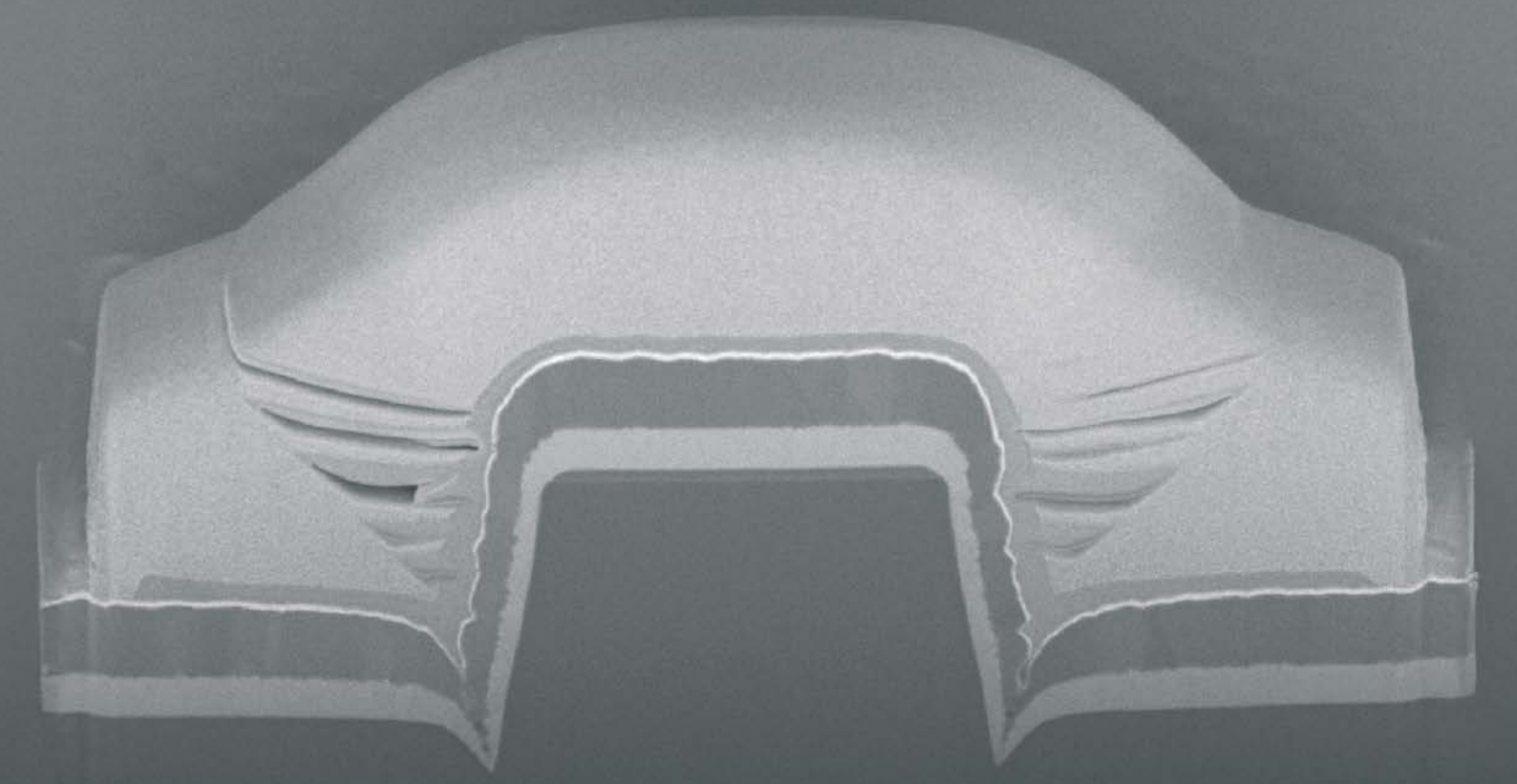


Watch the BAK 911 video

Want to know more about the Multi BAK?
Contact your local Evatec sales and service office to find out more.

Side Wall coverage – maximizing performance in new generation optoelectronic devices

Head of Business Field Compound & Photonics, ***Jakob Bollhalder*** explains why device side wall coverage is becoming important for thin film processes in Optoelectronic applications like Micro LED and how Evatec thin film solutions on CLUSTERLINE® can deliver just the performance required.



It's all about maximizing device performance

As device architectures get smaller, the output area of the device front surface gets smaller too, and that means that any light losses from side walls which would normally not be critical for larger devices start to represent a bigger and bigger proportion of the overall light output. But there are other factors to consider too! As device architectures shrink to 50 microns and lower, so does device volume to surface area ratio. Protecting the device by effective side wall coverage becomes important to avoid device performance degradation and maximize lifetime.

Figure 1a: CLUSTERLINE® 200 equipped with single process modules and FOUP

Figure 1b: CLUSTERLINE® 200 BPM equipped with Batch Process Module

CLUSTERLINE® 200 is the solution

Evatec's CLUSTERLINE® family is already a proven workhorse in the optoelectronics industry for applications including Micro LED, Mini LED and Edge-emitting Lasers (EELs). Processing of 200mm wafers either direct or on carriers makes it a flexible choice for sputter deposition of metals, TCOs, DBRs and passivation layers. Cassette-to-cassette configuration eliminates manual handling avoiding the risk of wafer breakage and reduces particles to the levels essential for high yield production of small scale devices. Different typical system layout for applications in optoelectonics are shown in Figure 1 for either single substrate or batch processing. Systems can be equipped with Advanced Process Control techniques like GSM broadband optical monitoring for layer termination and PEM plasma emission monitoring for control of film stoichiometry and maximizing deposition rates according to customer process. The systems are equipped with Evatec's proprietary cathode technology to deliver optimized side wall coverage.

Characterizing side wall coverage process performance

Every customer has their own unique device architectures and process requirements. Mapping performance of our tool and processes helps us be ready for whatever requests come our way. Figure 2 shows how we typically map side wall coverage performance on 8 inch substrates using a series of structures – pillars, trenches or vias of different dimensions.

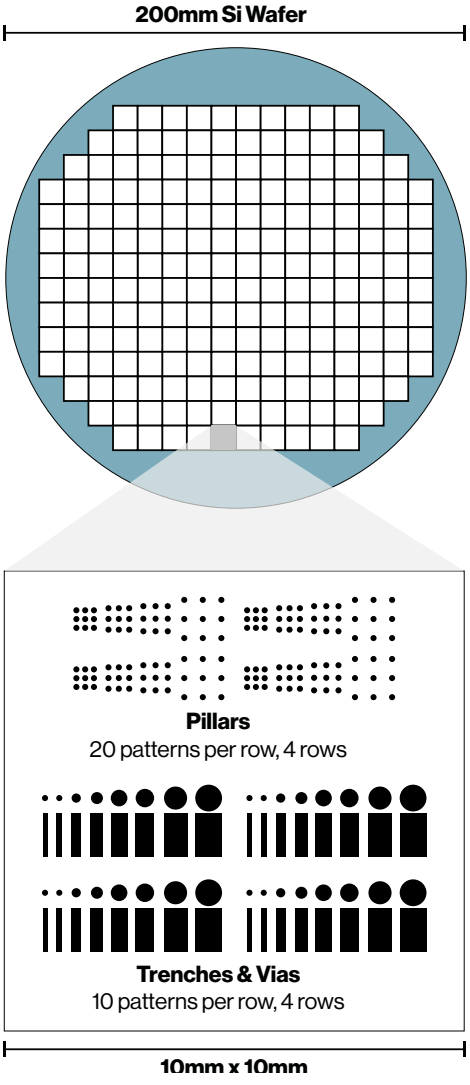


Figure 2: Side wall coverage performance test structures on wafer

Results so far

MicroLED technology

Figure 3a shows the architecture of a typical Micro LED while Figure 3b shows the excellent side wall coverage for ITO and metal layers when deposited on test structures using Evatec's propriety cathode technology.

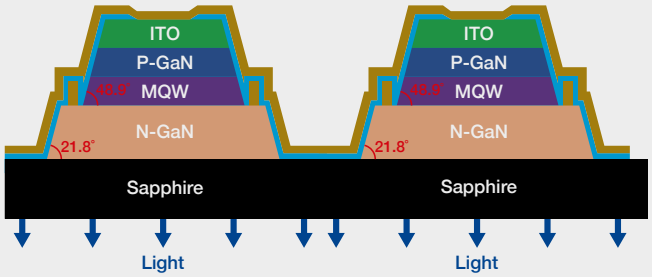


Figure 3a: Typical MicroLED architecture with side wall coverage for improved light extraction efficiency and passivation layer for device protection

EEL technology

MicroLED is just one area where innovations in coating processes for side wall coverage can be beneficial. New wafer level manufacturing approaches for edge emitting lasers eliminate the need for the processing of so called "laser bars" within complex mechanical jigs. Diode structures can be created within the wafer itself by lithography, etch and deposition stages and can then can have opposing facets (side walls) coated with the required high reflectivity (HR) or antireflection (AR) coatings whilst still at wafer level.

Figure 4 illustrates a typical process flow for EEL manufacturing according to two different manufacturing methods. In a traditional approach so called laser bars have to be assembled in a jig, coated on the first side then flipped and coated on the second side. In the Wafer Level Approach, photo-lithograph and etch steps are followed by coating steps to prepare devices over the whole wafer before final testing and dicing.

Traditional approach

*In a **traditional** approach so called laser bars have to be assembled in a jig, coated on the first side then flipped and coated on the second side.*

Wafer level approach

*In the **Wafer Level** approach coating technology for effective side wall coverage enables elimination of complex tooling and reduces overall process complexity.*

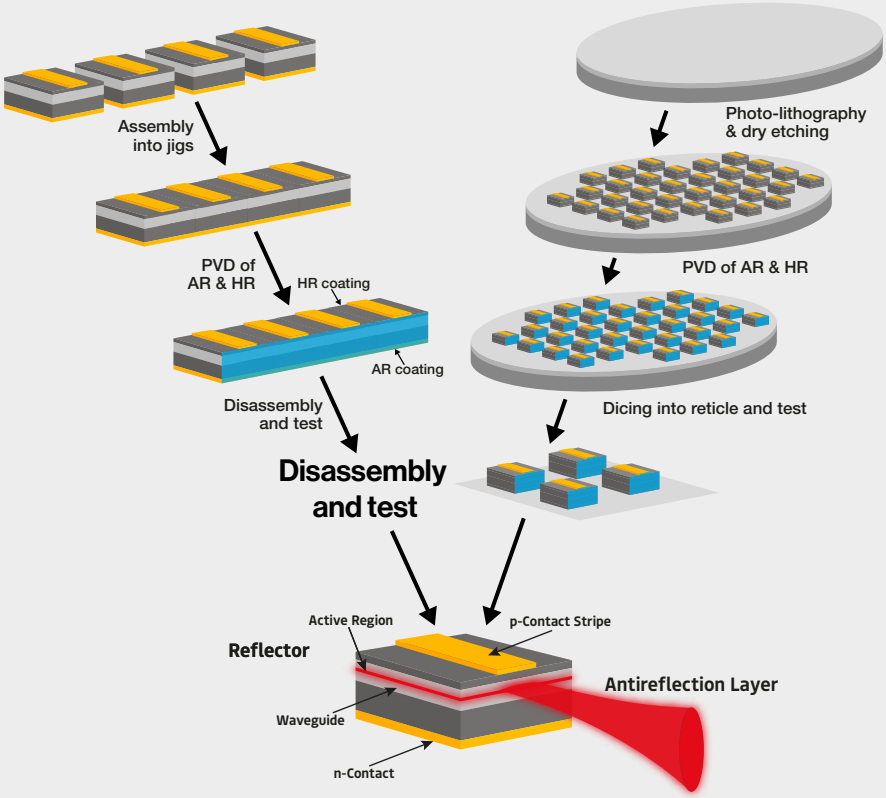


Figure 4: Typical process flow for EEL manufacturing

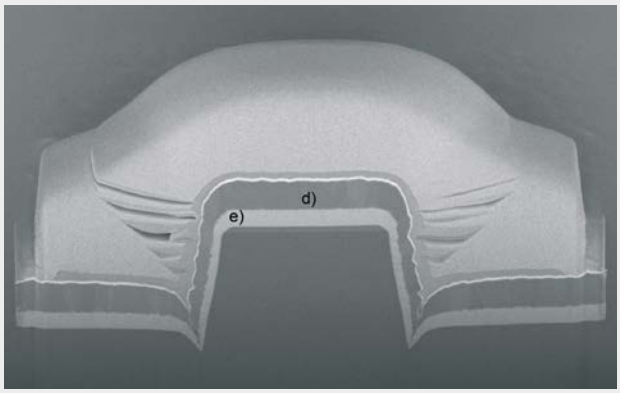
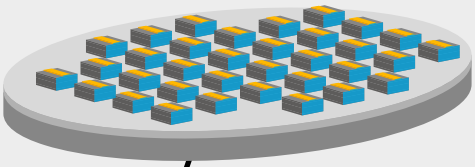
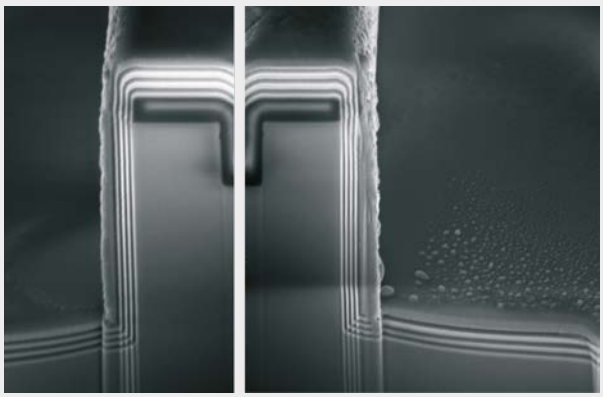


Figure 3b: Test structure deposition – d) Evatec Al; e) Evatec ITO



After PVD of AR & HR



- Same result for both active sides
- Clear and smooth layer separation
- Equal single layer thickness on side wall
- Side wall coverage 60% of top thickness

Want to know more?

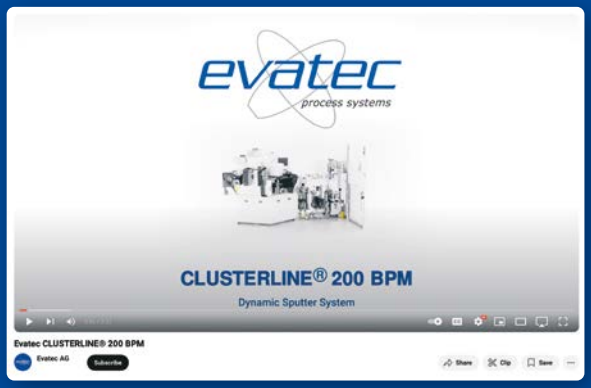
Our applications team would love to talk to you about the work we have been doing and find out how new approaches can support your own efforts in driving down manufacturing costs or improving process performance.

Contact us via your local Evatec sales and service office for more information
https://evatecnet.com/about-us/sales-service/

CLUSTERLINE® Family

YouTube

CLUSTERLINE® 200 BPM



YouTube

Hybrid DBRs – One process change brings two benefits for Micro LED production

Evatec Senior Product Marketing Manager ***Dr. Chongqi Yu*** talks about Evatec's latest process developments in Micro LED technology delivering both, 1 the lower cost of ownership and 2, the more compact structures that will help drive growth of mass market applications exploiting the benefits of Micro LED technology.

Micro LED – The benefits are clear

The performance advantages of emerging Micro LED including excellent brightness, contrast, and viewing angle are already well documented (Figure 1), but that doesn't mean we don't need to support our partners around the globe with process innovations that enable the introduction of the technology across mass market applications including Augmented Reality in 2025 and beyond.

Micro LED technology and production trends reported by both leading players in the industry and confirmed by analysts like Yole Group are calling for both smaller and smaller device sizes and the lowering of manufacturing costs. Production on larger wafer sizes is just one aspect driving down manufacturing costs but the introduction of so called "Hybrid DBR" process technology is an exciting next step with double benefits, on one hand enabling thinner structure / total device thickness and on the other reducing the normal process times for DBR deposition.

"Hybrid DBR processes – Increasing wafer throughput by 50% and reducing the total thickness by half"

MicroLED vs. OLED and LCD

	LCDs	OLEDs	MicroLEDs
Energy consumption	Medium	Medium	Medium to Low
Pixel density	Up to 1000 PPI	Up to 4,000 PPI (RGB for micordisplays)	> to 20,00 PPI monochrome demonstrated >4,500 PPI RGB demonstrated
Brightness	High (3000 nits peak on commercial TV)	Lowest [1]	Highest (up to 10^6cd/m^2 for microdisplays)
Contrast	Low to medium	High (true black)	Very high (true black + high brightness)
Color gamut	Wide with QDs	Wide with filters, resonant cavities	Wide (better with QD color conversions)
Lifetime	Good	Medium	Best
Environmental stability	Good	Medium with appropriate encapsulation	Best
Operating temperature	-40ºC to 100ºC	-30ºC to 85ºC	-100ºC to 120ºC
Switching speed	Low - ms	High - µs	Very high - ns
Viewing angles	Low to medium	Medium to high	High
Flexibility	Low	High	Medium
Maturity	High	Medium	Low
Cost	Low	Medium	High (2022)

Figure 1: Comparison of competing display technologies in consumer applications (Courtesy of Yole Group)

DBRs – Choosing the right thin film production platform architecture as a starting point

Process yield is also one of the significant drivers in driving down manufacturing costs, and that means using fully automated cassette-to-cassette processing for the lowest particle levels. But that's not the end of the story, the growing demand for sputter technology, with its higher film densities and process stability offers the potential for the best process repeatabilities.

Evatec's CLUSTERLINE® 200 BPM is already established as an industry standard sputter solution in the LED business for deposition of low damage TCOs and now its time to use the latest hybrid DBR process solutions for driving down manufacturing costs and thinning down the total layer thickness for high performance reflector layers too. A typical tool layout for Hybrid DBR processes is shown in Figure 2.

Hybrid DBRs – More throughput and thinner total thickness without compromize in optical performance

Hybrid DBR process technology delivers the required optical performance by combining a dielectric stack with a metal layer on either front or backside according to the Micro LED manufacturers preferred architecture. Less layers means shorter process times, higher throughputs and smaller scale device architectures. The typical RGB optical performance for Hybrid DBRs combining traditional dielectric stack with a silver layer is show in Figure 3.

In Figure 4 we see a comparison of overall stack thickness, process time and throughput for hybrid vs traditional sputtered DBRs on Evatec's CLUSTERLINE® 200 BPM configured for 8 inch processing. Throughput can typical be enhanced by 50% or more across all colours on 6 or 8 inch processing, and the total layer thickness of the mirror can be reduced by 50%. The results reported in Figure 4 are for hybrid DBRs utilizing silver, but for those customers preferring aluminium we can offer process solutions too – all you need to do is ask!

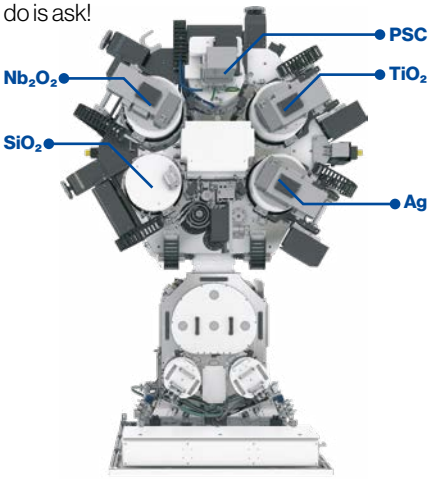


Figure 2: CLUSTERLINE® 200 BPM equipped with up to 5 process modules for depositon or etch or optical thin films with advanced process control technologies including broad band optical monitoring and plasma emission monitoring.

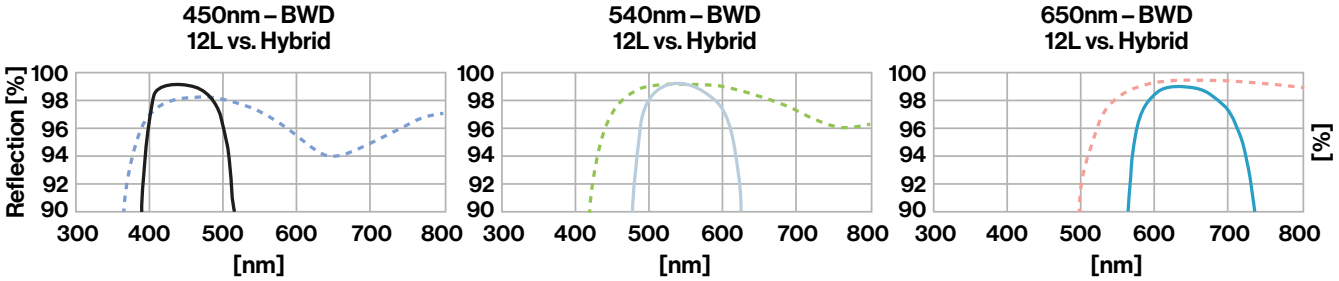
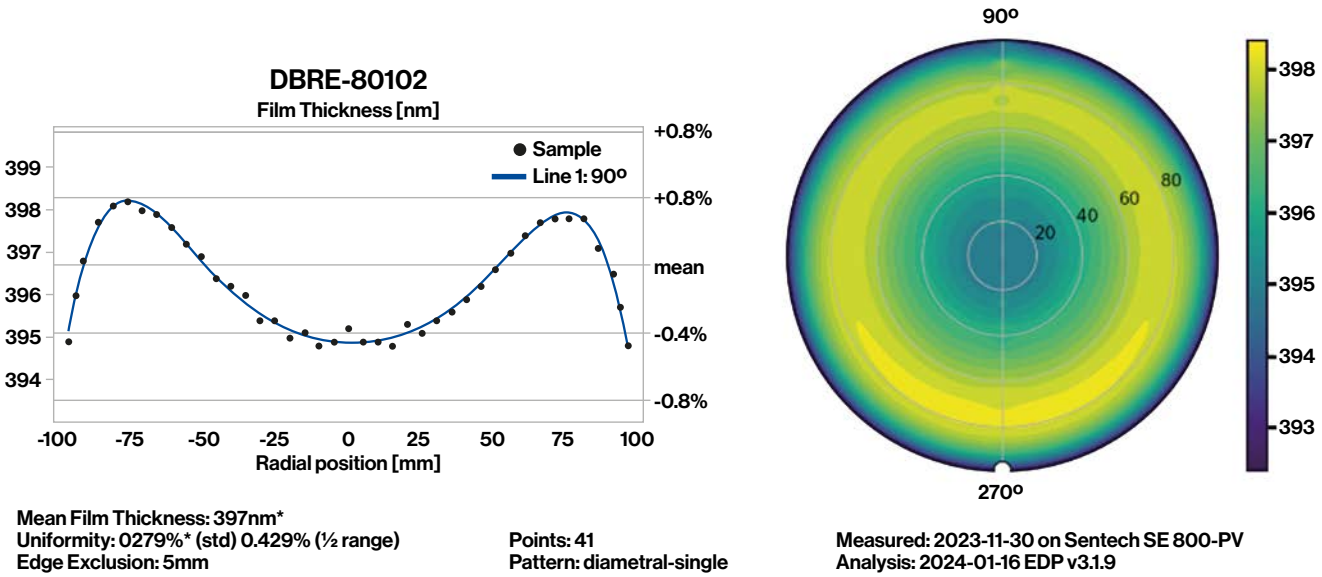


Figure 3: Optical performance of Hybrid stacks (- - -) for blue, green and red vs traditional DBRs (—)

	Blue – 450nm		Green – 540nm		Red – 650nm	
	12L	Hybrid 5L	12L	Hybrid 5L	12L	Hybrid 5L
End layer	SiO_2	Ag incl. Capping	SiO_2	Ag incl. Capping	SiO_2	Ag incl. Capping
Number of dielectric DBR layers	12	4	12	4	12	4
Total thickness (including Capping)	797.4 nm	529.8 nm	987.3 nm	586.96 nm	1177.2 nm	622.02 nm
Process time (tool time w/o handling) + Ag Capping	01:11:23	00:38:32	01:20:53	00:41:33	01:30:43	00:43:10
Resuts Sputtering on D263						
Max Reflectivity @nm	99.33% @ 437nm	98.90% @ 461nm	98.99% @539nm	99.30% @ 552nm	98.77 @ 637nm	99.54% @ 664nm
Reflectivity @nm – (Bwd)	99.23%	98.85%	98.96%	99.26%	98.65%	99.50%
Range of Reflectivity	>98% @ 405-483nm >99% @ 417-463nm	>98% @ 399-554nm	>98.8% @ 517-556nm	>99% @ 487-622nm	>98% @ 597-678nm	>99% @ 553-819nm
Stopband width	78nm @98% 46nm @99%	155nm @98%	39nm @99%	135nm @99%	81nm @98%	266nm @99%
Throughput 8"						
Substrates / h	9.1	13.7	8.2	13.1	7.5	12.6
Substrates / month (48 weeks/y, 85% uptime)	5198	7825	4684	7483	4284	7197
Throughput 6"						
Substrates / h	12.1	17.6	11	16.9	10	16.4
Substrates / month (48 weeks/y, 85% uptime)	6912	10053	6283	9653	5712	9368

Figure 4: Comparison of throughput for standard vs hybrid DBR



Mean Film Thickness: 397nm*
Uniformity: 0279%* (std) 0.429% (½ range)
Edge Exclusion: 5mm

Points: 41
Pattern: diametral-single

Measured: 2023-11-30 on Sentech SE 800-PV
Analysis: 2024-01-16 EDP v3.1.9

Figure 5: Deposition uniformity of SiO_2 on CLUSTERLINE® 200 BPM < ± 0.5% over 8 inch.

Base system performance is key

The benefits of reduced process times, high deposition rates and enhanced throughput can only be achieved if base system performance including deposition uniformities and run to run process repeatability meet the required Micro LED standards. CLUSTERLINE® 200 BPM uses advanced process control (APC) technologies including in-situ broadband optical monitoring (GSM) of the substrate itself plus plasma emission monitoring (PEM) combined with dynamic sputter architecture without shapers to deliver the levels of process control required.

Figure 5 illustrates typical film thickness uniformity for deposition of dielectrics of better than ± 0.5% on 8 inch.

Figure 6a shows typical wafer in wafer, wafer to wafer and run to run repeatabilities on 6 inch of less than ± 0.6%. Figure 6b shows optical performance repeatability.

Material	Layer thickness	Thickness uniformity $U(Max\ Min)\ [\pm\%] = \frac{(Max - Min)}{2 \cdot Avg} \cdot 100$		
		WiW	WtW	RTR
SiO_2*	300nm	<±0.5%	<±0.5%	<±0.5%
Nb_2O_5*	300nm	<±0.5%	<±0.5%	<±0.5%
TiO_2*	300nm	<±0.5%	<±0.5%	<±0.5%

**with rotating Chuck, PEM & GSM*

Figure 6a: Deposition uniformity achievements for single layers on 6" substrates

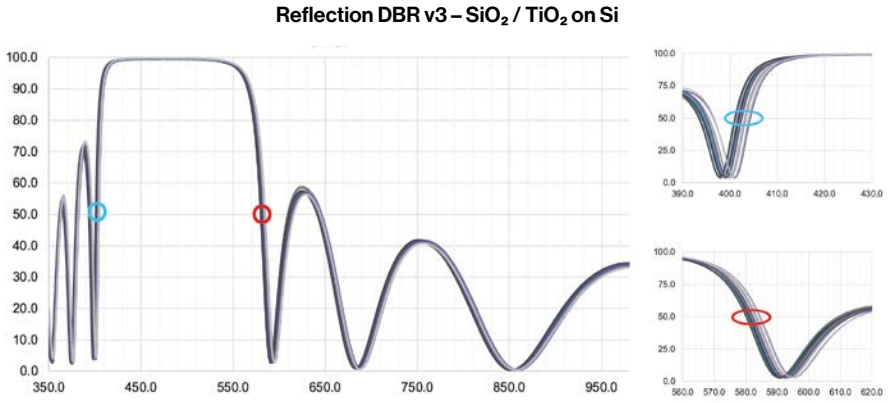


Figure 6b: Optical performance repeatability

How can we help you?

Every manufacturer has different device architectures and therefore requirements. Our LED process specialists are here to help not just with DBR solutions but also with metals and TCOs too.
Contact your local Evatec sales and service office to find out more.

A view from Yole Group

As OLED keeps improving, Apple's withdrawal increases sense of urgency for MicroLED commercialization

Apple created the MicroLED industry when it acquired startup Luxvue in 2014. It then spent ten years and $3 billion developing the technology. If it hadn't been for that keen interest, the enthusiasm since shown in MicroLED by most OEMs and display makers would have been much more subdued.

Osram completed a $1.3 billion 200 mm MicroLED fab to meet Apple's needs, and an Apple watch was scheduled for release in 2026. But in February 2024, Apple canceled the project, sending shockwaves into the industry and seriously undermining its prospects. Two years ago, this could have been the death of MicroLED. However, Yole Group believes it has now gained sufficient momentum of its own to keep going.

Exiting 2023, the industry had spent $12 billion in MicroLED directly and another $2 billion in M&As. About 40% of that total is related to Apple. Yet, other players have spent $7 billion non-related to Apple's efforts. MicroLED remains critical for the long-term strategies of Taiwanese companies such as AUO. The ecosystem is strengthening further, and MicroLEDs had a strong showing at the recent Touch Taiwan and Display Week industry events.

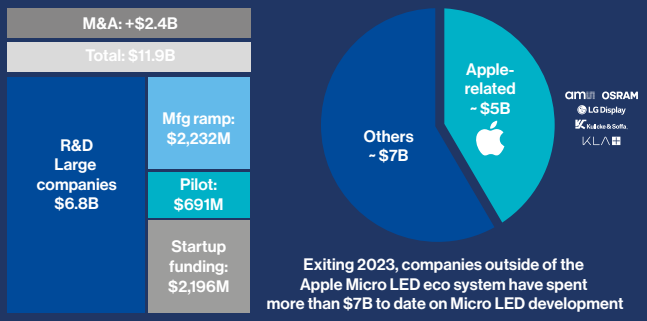
To succeed, MicroLED must reach a similar cost structure to OLED while delivering strong performance differentiation. With Apple gone, MicroLED will focus on applications with clear differentiation against OLED: AR, automotive, and various specialty applications such as transparent displays. Smartwatch forecasts are cut drastically but remain the low-hanging fruit for MicroLED in terms of consumer applications. AUO started shipping small volumes for luxury watches.

Despite Apple's project cancellation, there's still good momentum, but also a sense of urgency to accelerate commercialization. With Apple gone, the central question is how to incubate the industry. Can low-volume smartwatches, automotive, and various niche applications bootstrap the industry to achieve the economies of scale required to enable higher-volume consumer applications? This is reminiscent of OLED's situation until 2007, when Samsung bit the bullet and built the first AM-OLED fab, at a time when benefits compared to LCD were still very questionable. That's what the industry was hoping Apple would do for MicroLEDs.

The next 18 months will be critical. Will Samsung remain committed to MicroLED TVs? Can other champions emerge? For now, the industry's center of gravity has shifted toward Taiwan, but China could once again surprise us.

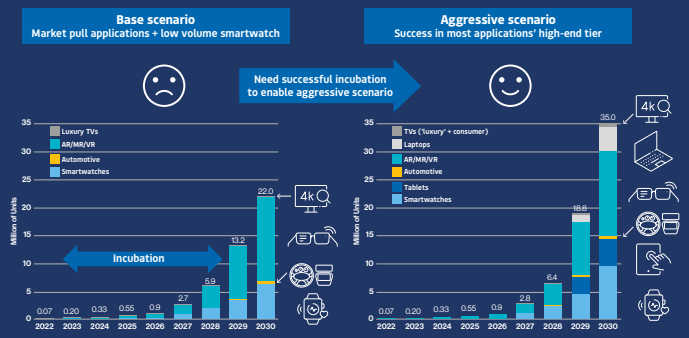
Micro LED development and industrialization effort

Source: Micro LED 2023 report, Yole Intelligence – June 2024 update



Consumer MicroLED volume forecast - intermediate 2024 analysis

Source: MicroLED 2023 report, Yole Intelligence – June 2024 update



YOLE Group

About the author

As Principal Analyst, Display at Yole Group, **Eric Virey, Ph.D.**, is a daily contributor to the development of LED, OLED, and display activities. He has authored an extensive collection of market and technology products as well as multiple custom consulting projects on subjects including business strategy, identification of investments or acquisition targets, due diligence in buying and selling, market and technology analyses, cost modeling, and technology scouting. Thanks to his deep knowledge of the LED/OLED and display industries, Eric has spoken at more than thirty industry conferences worldwide over the last five years. He has been interviewed and quoted by leading media all over the world. Eric Virey holds a Ph.D. in Optoelectronics from the National Polytechnic Institute of Grenoble.

Metalenses – a world of opportunity

Metalenses are tiny optical elements that can manipulate light like traditional lenses, but their small size, and "flat" architecture offers the potential for cost-effective manufacture at large scale using a "wafer level optics" approach at substrate sizes up to 12 inch. Senior Product Marketing Manager ***Dr. Clau Maissen*** explains how Evatec process know-how is helping customers deliver the sputtered layer qualities and process repeatability required for mass market applications

A technology with huge potential

Metalenses are at the forefront of optical innovation, transforming the way we manipulate light with their ultra-thin, flat structures. Unlike traditional bulky lenses, metalenses utilize nanostructured surfaces to precisely control light, offering unprecedented advantages in miniaturization and performance. This breakthrough technology is poised to revolutionize a wide range of applications, from enhancing the imaging capabilities of smartphone cameras and augmented reality glasses to advancing medical imaging devices with greater precision and clarity. Figure 1 illustrates how a traditional optical assembly can be simplified significantly using a metalense approach.

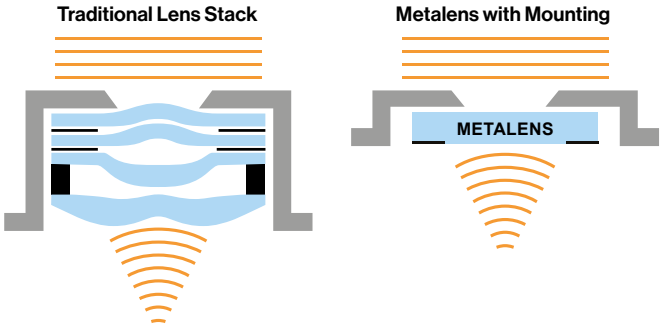


Figure 1: Metalens enable simplification

Thin film technology and wafer level optics are key

Evatec's expertise in the deposition of high-index material layers plays a crucial role in the fabrication of these advanced lenses, ensuring the uniformity and repeatability needed for high-performance optical systems. By leveraging Evatec's specialized processes, manufacturers can achieve the exacting standards required for mass-market adoption of metalenses, paving the way for a new era of optical technology.

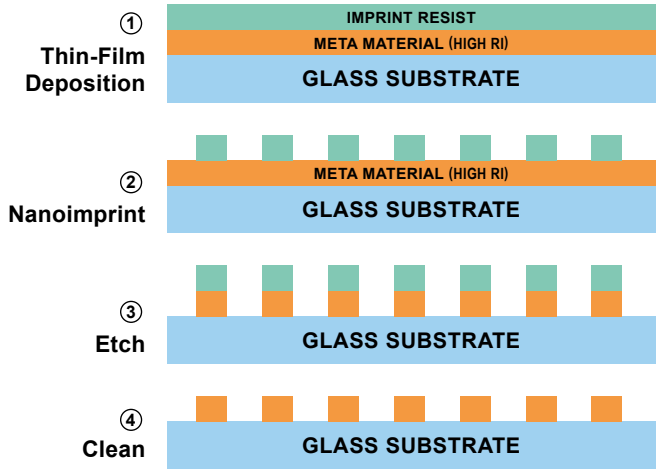


Figure 2: Example manufacturing process flow

A key advantage of metalens technology is the ability to start from a wafer. Following deposition of a high index material such as amorphous Si or metal oxides, manufacturing technologies such Nanoimprint and etch are then used to create the functional pillars "so called metaatoms" at the heart of the device. AR coatings and encapsulation layers then follow before the whole wafer is then diced to give final individual devices. Figure 2 illustrates a typical process flow.

The high index materials (e.g. amorphous hydrogenated Si for Near IR, Nb_2O_5 for visible) and pillar architectures will of course vary according to application and operating wavelength requirements. Irrespective of the application however, the ability to deposit highly uniform repeatable films of the index material up to 12 inch substrates is key.

Evatec know-how for deposition of high index materials

Evatec has long know-how in sputter deposition of high index materials on both its MSP and CLUSTERLINE® 200 BPM platforms. Use of advanced process control technologies like plasma emission monitoring ensures correct stoichiometry and high deposition rates whilst GSM optical broadband monitoring delivers precise film thickness. Typical deposition results on 8 and 12 inch substrates are shown in Figures 3a & 3b.

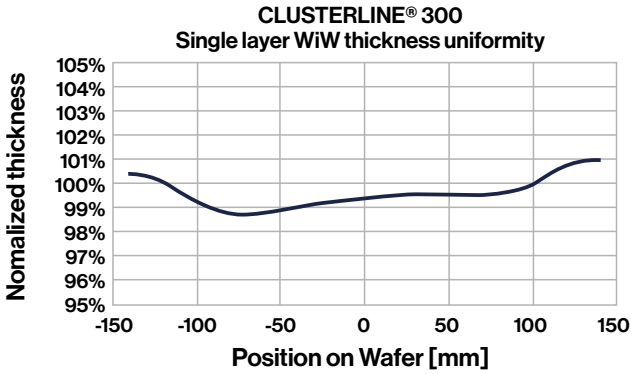


Figure 3a: aSi:H on CLUSTERLINE® 300 thickness uniformity

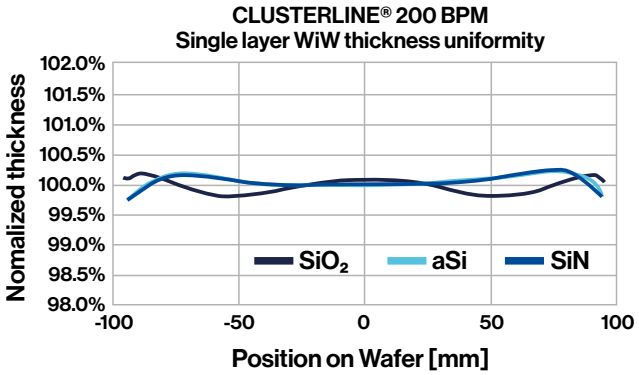


Figure 3b: SiO_2, aSi, SiN on CLUSTERLINE® 200 BPM thickness uniformity

Images in Figures 1 and 2 plus cover image courtesy of Moxtek.

Control of particles is key

Single particles can have an impact on the performance of a lens over an area up to 10x larger than the particle itself depending on the technology used to fabricate the lens. So particle control is key. Tools like Evatec's MSP or CLUSTERLINE® family which eliminate uniformity shapers from the sputter system not only enable higher deposition rates but also eliminate a significant source of particles too.

For those customers with even more demanding particle specifications the automated cassette-to-cassette handling systems of CLUSTERLINE® can improve further particle managment even more. Figure 4 illustrates typical particle data for single layer deposition on CLUSTERLINE® 300.

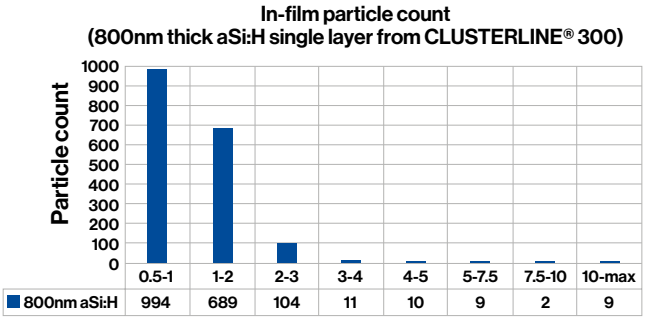


Figure 4: Particle data of single layer aSi

Want to know more?
For more information about Evatec coating solutions for metalense applications contact your local Evatec sales and service office at:
https://evatecnet.com/about-us/sales-service/

MOXTEK®

About Moxtek*

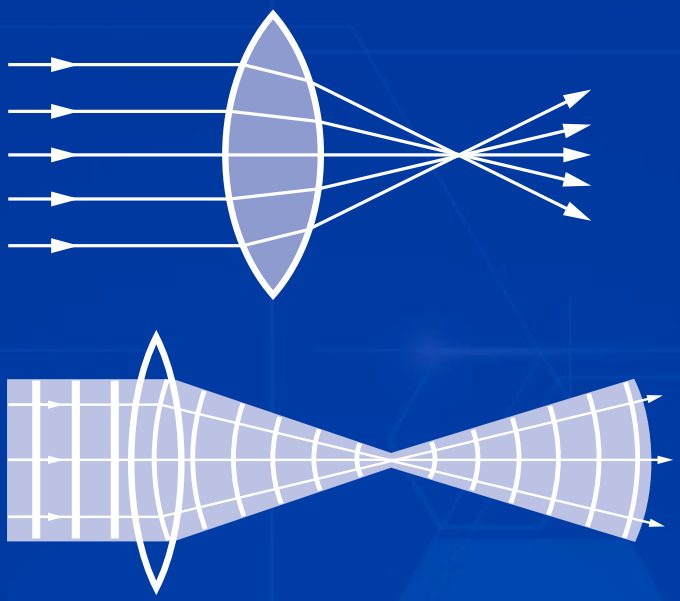
MOXTEK® is a leading developer and manufacturer of advanced nano-optical and x-ray components used in display electronics, imaging, and analytical instrumentation. Moxtek produces high volume, innovative, solution-based products that enable many new scientific discoveries and improve the quality of everyday life. Moxtek manufactures functional metasurfaces including: metalens, patterned nanostructures, Meta-Optical Elements (MOE), Diffractive Optical Elements (DOE), waveguides, photonics crystals, and biosensor arrays. Please visit their website to learn more.

For more information visit **https://moxtek.com**

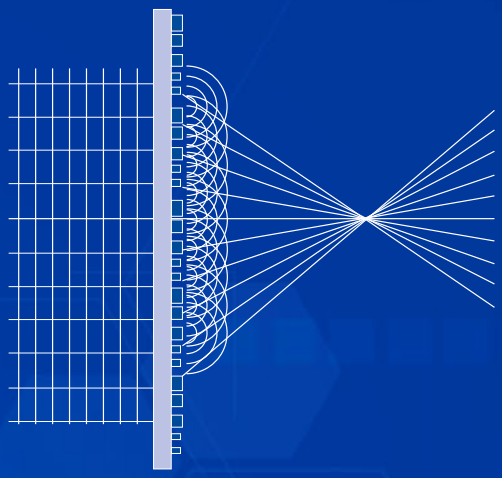
*Source: Moxtek website

SPOTLIGHT ...METALENSES

An introduction to Metalenses



Left: Conventional refractive lens: refraction at the interface between air and lens directs the light to a focal point. Another view to the same effect is: a plane wave is converted to a spherical wave.



Right: Shows a metalens. A plane wave is converted to a spherical wave via the response of nanostructures (nanoantennas) built on the surface of the substrate. The surface is a quasi-periodic structure with subwavelength dimensions.

Metalenses – Potential benefits

Benefit		
Miniaturization	✓	Metalenses allow for the creation of smaller, lighter optical devices, which is especially beneficial for applications in consumer electronics such as smartphones and AR glasses. For instance, Samsung is researching metalenses to integrate into their smartphone cameras, aiming for improved image quality and reduced lens size. Similarly, Apple is reportedly investigating the use of metalenses for future iPhones and AR glasses to achieve superior optical performance and device miniaturization .
Smaller optical packages with more functionality	✓	Meta Optical Elements (MOEs) enable the development of smaller optical packages with multiple functions , making them ideal for compact devices with advanced optical requirements. This multifunctionality is particularly advantageous in compact devices where space is at a premium.
Reduced complexity and cost of optical assemblies	✓	Metalenses simplify optical system design by reducing the number of elements required since metalenses do not suffer from spherical abberation, thereby lowering the overall cost and complexity of optical assemblies such as camera lenses. Unlike traditional lenses, metalenses are less sensitive to alignment issues, which simplifies manufacturing and assembly processes.
High Numerical Aperture (NA)	✓	Metalenses achieve high NA values, which are crucial for applications requiring high resolution, such as microscopy and high-end cameras.
Thermal stability	✓	They exhibit high thermal stability, essential for high-power laser systems and harsh environments.
Polarization control	✓	Metalenses can be engineered to control the polarization state of light, beneficial in optical communication and sensing applications .
Reduction of chromatic aberrations	✓	Chromatic aberration can be an issue with metalenses, but newer approaches have significantly reduced these aberrations. Advanced designs enable metalenses to achieve high Numerical Aperture (NA), improving image clarity and color accuracy.

Europe – A powerhouse in III-V solar cells manufacturing

Evatec Europe Sales Manager, ***Frank Wette*** and Head of Sales Europe ***Sandro Bertelli*** explain how Evatec evaporation solutions on the BAK and the latest substrate handling options are helping customers deliver the process repeatabilities and high production yields essential for successful manufacture of III-V solar cells.

Why III-V semiconductors for space applications?

III-V semiconductor-based photovoltaics play a crucial role in space applications due to their unique properties. Here are just some of the reasons why III-V solar cells are favoured for use in space:

- **High Efficiency:**
  III-V multi-junction solar cells exhibit exceptional efficiency compared to traditional silicon-based cells. For instance, a combination of InGaP with a bandgap of 1.9 eV, InGaAs with a bandgap of 1.4 eV and Ge with a bandgap of 0.7 eV allows III-V cells to absorb a broader range of photons at energies close to the individual bandgaps, making them highly efficient. Higher efficiency translates to smaller arrays, reduced weight, and increased payload capacity for spacecraft.
- **High Voltage:**
  Due to the serial combination of several III-V semiconductor absorbers within a multi-junction solar cell, the output voltage of an individual cell rises considerably. The high thermal stability of the III-V cell voltage compared to Silicon allows for the design of relatively short solar cell strings on a satellite panel, making the solar array design more flexible and reliable.
- **Radiation Resistance:**
  Space environments expose solar cells to cosmic radiation, which can degrade their performance. III-V materials have demonstrated superior radiation resistance compared to other materials. Additional concepts, such as distributed Bragg reflectors (fully patent protected by AZUR SPACE) within the semiconductor stack further enhance the radiation resistance of the III-V solar cell devices. They maintain efficiency even in harsh conditions.
- **Space Heritage:**
  III-V solar cells have been widely used in space systems for decades. Their reliability and proven track record make them a trusted choice.

In summary, III-V-based solar cells offer a compelling combination of efficiency, radiation resistance, and historical success in space applications. Their lightweight and flexible nature make them ideal for powering satellites and spacecraft.

Thin film process repeatability is key

Of course each manufacturer has their own cell designs and process requirements but Evatec typically supports customers with process solutions for deposition of either dielectrics for antireflection coatings or with process solutions for metals. The high added value of typical 6 inch substrates prior to coating call for both coating systems and processes that are robust for the reliable and stable repeatable deposition of layers without failures. Secure wafer handling is needed to eliminate risk of substrate damage and even breakage and coating process technology itself needs to avoid substrate damage due to stray electrons / ions.

Europe – A solar cell production powerhouse

We are very happy that our European region already has a number of well-established manufacturers including **AZUR SPACE** and **CESI** supporting a strongly growing global market.

AZUR SPACE
A 5N PLUS COMPANY

"More than 11 MW space qualified solar cells & CICs in space"
www.azurspace.com

CESI
Inspired with innovation

"Enabling four junction cells with space efficiencies beyond 35%"
www.cesi.it/space-solar-cells

The BAK Evaporator Family – A long history and an exciting future

The original BAK evaporator concept may well be 50 years old but its flexible tool architecture combined with modern process source and control technology enables customers to manage manufacturing and recording of actual production process data according to the strict standards of the solar industry.

BAK platforms are currently available in a range of sizes from 0.5 to 1.4 meters optimized according to customer's substrate size, batch processing size and throughput. The layout of a BAK1101, a typical size used by the solar industry, is shown in Figure 1. In addition to the usual e-gun technology there is plenty of space for integration of additional equipment such as plasma sources plus process accessories like heating. Platform control and process data logging is managed by Evatec's Khan and a host integration option gives customers the control they need within the fab.

Whilst the solar cell industry may call for rigorous long term process repeatability and stability of the manufacturing environment that doesn't mean there is no appetite for improving efficiency. For many manufacturers the road to driving down costs involves the increasing use of automation for substate handling. Figure 2 illustrates how the latest generation of BAK evaporators can be equipped with a range of different semi or fully automated load options according to the substrate and platform size.

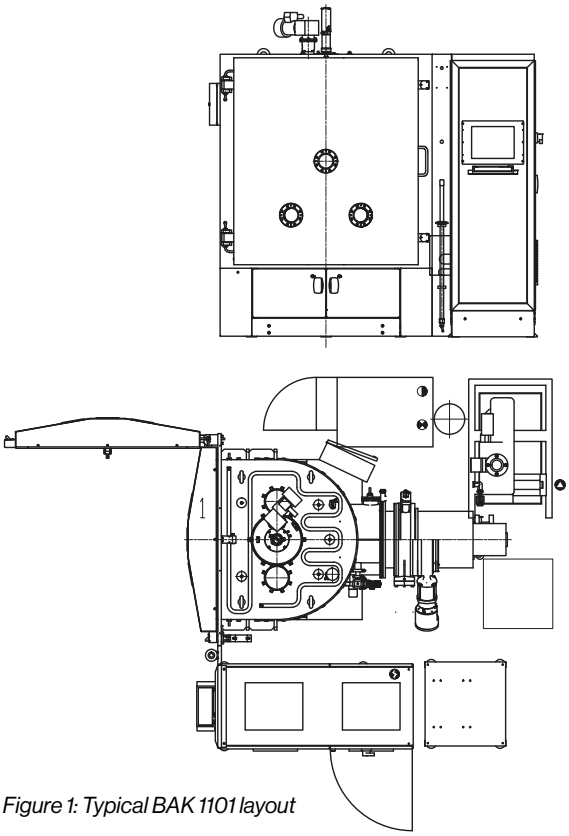


Figure 1: Typical BAK 1101 layout

A wealth of substrate handling options for the BAK family

Manual load / unload

- Either wafer direct to calotte in chamber or manual load of preloaded segment.

Semi automated

- Manual load of calotte-robot load / unload of calotte to chamber. Loading capacity per batch can be increased through unsegmented dome design.

Semi automated

- Manual load of calotte-robot load / unload of calotte to chamber via vacuum load lock. Reducing batch times through quicker unload / loading, faster pumping.

Fully automated

- Cassette-to-cassette (or FOUP to FOUP) via intermediate loadlock as featured on Multi BAK.

Increasing levels of handling automation

Figure 2: Semi or fully automated load options for BAK evaporators

Want to know more about the solar production solutions on the BAK platform?

Our application specialists would love to talk to you. Simply contact your local sales organization **https://evatecnet.com/about-us/contact-us/**

Access the latest brochure to learn more about the BAK family

Watch the Multi BAK video to learn how you can increase throughput and reduce energy costs

Quantized Nanolaminates through the microscope -

A step forward in optical thin film technology?

Evatec's Principal Scientist ***Dr. Silvia Schwyn Thoeny*** introduces quantized nanolaminates, tells us the potential benefits for optical thin film production and how they can be manufactured effectively by sputter technology on CLUSTERLINE® 200 BPM.

Why Quantized Nanolaminates?

Optical interference coatings such as anti-reflection, mirror or filter coatings are based on stacks of materials with at least 2 different refractive indices, n. The interference effect is stronger if the difference in refractive index between materials is larger. Hence, a stack design based on materials with a larger difference in refractive index requires a smaller number of individual layers and thus less overall thickness to fulfill the same specification as a design based on materials with a smaller difference. In addition to the refractive index, the materials have to fulfill other requirements, among those being transparency with negligible losses in the wavelength range of interest.

However, in dielectric materials the refractive index and absorption edge are linked. Materials with high refractive index have their absorption edge at a long wavelength, while low refractive index materials have the absorption edge at a short wavelength. TiO_2 is the dielectric material with the highest refractive index, which is transparent in the visible range of the spectrum starting to transmit at ca. 400 nm. Having a material at disposition with a higher refractive index while being transparent in the VIS would be of broad practical relevance, since it would allow interference designs with a lower number of layers and reduced overall thickness.

An approach to overcome the connection between the two characteristics is Quantized Nano Laminates (QNL). In this concept thin layers of high and low refractive index with a thickness in the nanometer range or below are stacked. The limited structure size leads to a change of the energy gap, which can be adjusted by the physical thickness of the materials, whereas the thickness ratio of the materials determines the effective refractive index of the QNL.

In optical interference coatings, the decoupling of band gap and refractive index potentially offers the advantage of using the QNL material combination instead of using a specific material. The stack structure of a typical coating with QNL in comparison with standard interference is illustrated in Figure 1.

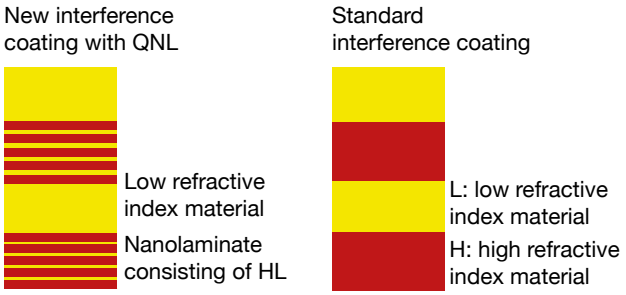


Figure 1: Comparison of film structure

As an example, in the UV range the band gap of Ta_2O_5 can be pushed towards shorter wavelength and can thus replace the use of HfO_2. This is desirable since hafnium targets are expensive and because HfO_2 has a tendency to form polycrystalline films with grain boundaries which can cause losses by straylight. Another very interesting material combination is QNL composed of amorphous silicon and SiO_2 which offers a higher effective index than TiO_2 with being transparent well into the visible part of the spectrum.

Nanolaminates Benefits

Table 1 summarizes the potential benefits of nanolaminates when it comes to optical thin film production. Key to commercial realization is finding a practical production technique and that's where sputtering comes in. Although ALD and IBS lead to good results, they do have drawbacks with regard to volume production, whereas magnetron sputtering achieves deposition rates comparable to standard optical thin film production processes.

Potential benefits of quantized nanolaminates
✓ Decoupling of refractive index and absorption edge
✓ Extending useful range of high index materials
✓ Improved film performance
✓ Comparable results achieved with less complex stacks / shorter process times
✓ Replacement of expensive materials
✓ In-situ PEM and optical monitoring can be used just like in classical processes

Table 1: Potential benefits of Quantized Nanolaminates

Now you really can 'have your cake and eat it'

Production solutions on CLUSTERLINE® 200 BPM

Evatec's CLUSTERLINE® 200 BPM dynamic sputter tool with its large substrate table is well suited to nanolaminates deposition. The deposition system has a capacity of 15 substrates of diameter 200mm. Substrate loading and unloading is executed automatically through a vacuum transfer module and load-lock. The system is also equipped with broad band and monochromatic optical monitoring.

For the deposition of aSi - SiO_2 QNL one sputter source was equipped with a silicon target with the purpose to deposit an amorphous silicon layer. The SiO_2 layer is formed by the plasma source (PSC), where the aSi film partially gets oxidized by the oxygen plasma. The plasma source is a RF-driven capacitively coupled discharge, where oxygen as operating gas is partially dissociated and ionized. The schematic tool configuration is shown in Figure 2.

When depositing the long pass filter consisting of aSi - SiO_2 QNL as the high refractive index material and SiO_2 for the low refractive index material, a second sputter station equipped with a silicon target was used to reactively deposit the low index SiO_2 layers.

The turntable configuration is perfectly suited for the deposition of QNLs. The substrates pass repeatedly beneath the active sources, thereby exposing the substrates to both the sputter (Si & Ta) and the plasma source with each rotation. The total thickness deposited in one turn is determined by the rotation speed of the table, a parameter which can easily be varied in a wide range, and the deposition rate. The thickness ratio of the aSi and SiO_2 materials is determined by the sputter and the plasma source power, which can be adjusted individually. Deposition rates for QNL layers tend to be as high as those for single aSi since the active source is run at standard conditions.

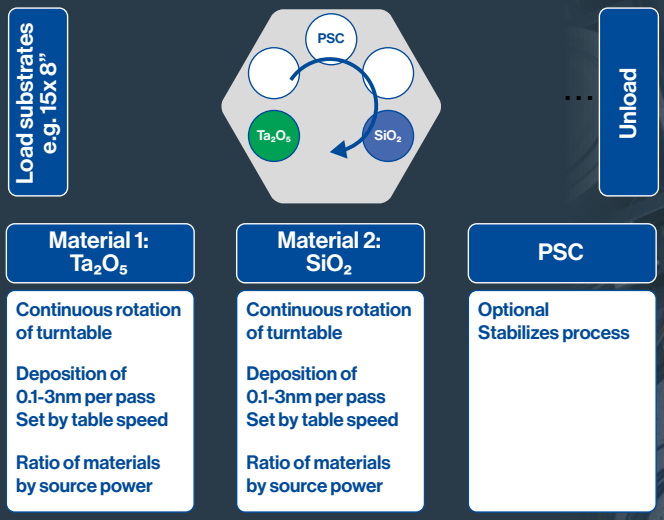


Figure 2: CLUSTERLINE® 200 BPM

Experimental results

1. Illustrating the quantized nanolaminate effect

In a first experiment, the Si and Ta sources were run at fixed powers. The table speed was varied from 3 to 15 seconds per pass, which means that the thickness ratio of high to low layers stayed constant, but the individual layer thickness increased with the slower table speed. The well thickness, i.e. thickness of Ta_2O_5 was determined to be in the range of 0.2-1 nm. According to the theory it was expected that the absorption edge would shift towards shorter wavelengths the thinner the individual well layers became, whereas the effective refractive index would remain constant for all five samples. This behavior was indeed seen in the transmission measurements. The absorption edge of the 3s/pass sample lies at the shortest wavelength, whereas the 15s/pass results in the longest wavelength edge with a difference of 18 nm between the samples (see Figure 3). For reference the absorption edge of a Ta_2O_5 layer is indicated by a dotted line. In the longer wavelength range above 280 nm, all curves overlay since they all have the same effective refractive index and optical thickness. Furthermore, they touch the solid line for ½ λ optical thickness indicating very low absorption of the QNLs in the longer wavelength range.

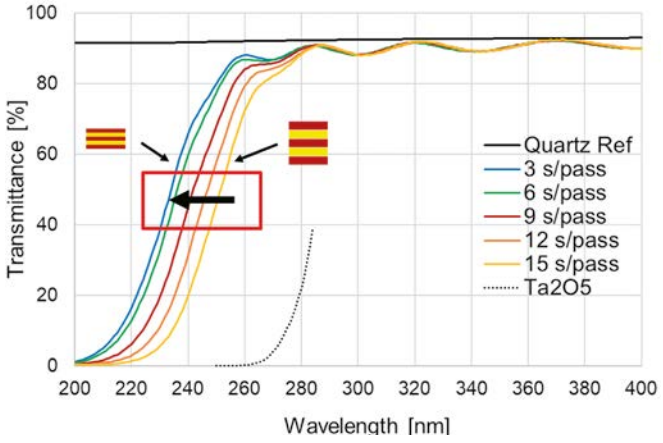


Figure 3: Transmittance of QNL layers with the same thickness ratio of Ta_2O_5 to SiO_2, but with increasing table speeds. The thinnest layers deposited with the highest table speed show the largest shift in absorption edge to shorter wavelength.

2. AR Coating

In a second experiment, a UV AR coating centered on 266nm was deposited on silica substrates using a stack comprising SiO_2 and QNL of TaO_2/SiO_2 showing an effective coating without the use of Hafnia. The reflectance and transmission performance on a double side coated sample are shown in Figure 4.

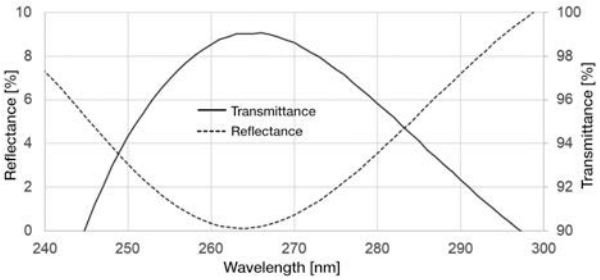


Figure 4: Transmittance and reflectance measurements of the antireflective coating of SiO_2 and QNL layers showing excellent transmission at 266 nm

3. Mirror at 355nm with short pass filter

Figure 5 shows a comparison of performance for two short pass filters: the curve in red is a standard SiO_2-Ta_2O_5 coating. Both designs reflect at 355nm and transmit light at shorter wavelength, but transmittance falls off rapidly below 300nm using standard filter designs whereas quantized nanolaminate structure enables significantly higher light output down close to 280nm.

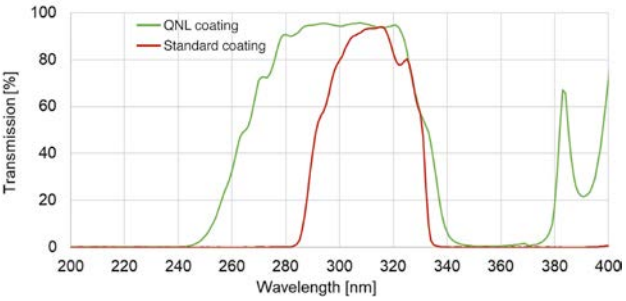


Figure 5: Short pass filter transmittance of a design using SiO_2-QNL (green) compared to standard coating (red) using SiO_2-Ta_2O_5

4. Long pass filter

In Figure 6 we see a comparison between long pas filters both having 16 layers. The classical design using TiO_2 / SiO_2 blocks only from 520 to 670nm and would require twice the number of layers to give equivalent performance to the QNL design using aSi/SiO_2. This shows how QNL structures can reduce overall coating thickness, deposition times and manufacturing costs.

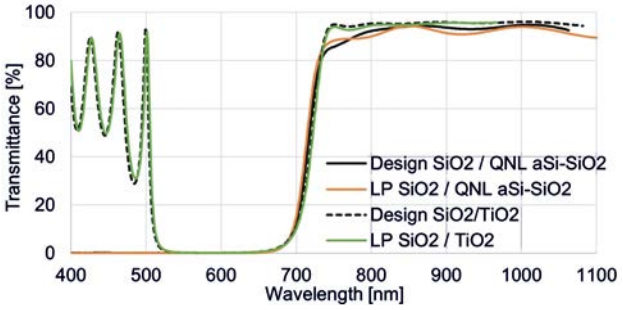


Figure 6: Transmittance of a long pass filter based on SiO_2/QNL aSi-SiO_2 and on SiO_2-TiO_2 for comparison

Quantized nanolaminate: the theory

In standard dielectric materials the refractive index and the energy of the absorption gap are fundamentally linked. Quantized nanolaminates however allow us to set the refractive index and the absorption edge independently within the limits given by the bulk properties of the high and low index material.

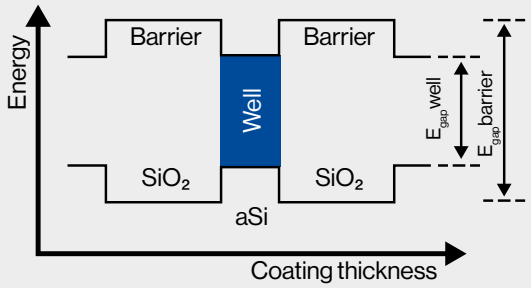


Figure 7: Periodic structure of high and low band gap areas, which limit the electron mobility

The theory of the quantized nanolaminates has already been detailed in other publications but here is a quick summary. As already mentioned, optical coatings mostly produce amorphous or polycrystalline materials whose band structure is not clearly defined, nevertheless an energy gap between quasi-free ground states and higher conduction states is present. Thus, the band gap itself can be regarded as a depletion zone of states and the densities between bound and free states are so low that they can be neglected. Thus, the potential well, which is necessary for the quantization is clearly defined.

The electron mobility can be limited in the growth direction if two materials with high and low band gap are combined in a thin periodic structure. In this case the low index material will act as a barrier, whereas the high index material acts as the quantum well, as illustrated in Figure 7. Since this is a simple potential consideration, even non-closed atomic layers can lead to a suitable periodic potential.

The thickness of the quantum well will determine the shift in band gap, whereas the thickness ratio of high to low bandgap material will determine the refractive index. Thus, the novel concept of so-called quantizing nanolaminates (QNLs) allows for independent adjustment of the optical band gap and the refractive index. To give an idea of the thicknesses required we turn to data published for SiO_2-Ta_2O_5 which shows that the quantum well layers should be much smaller than 2 nm to achieve a shift which is of practical use.

Please take a look at the open access paper published in *Optics Express and Advanced Photonic Research* to access more references of previous work reported in the literature about Quantized Nanolaminates and more results for the work being done at Evatec.

Come and talk to us

Our application engineers are ready to share more results and to collaborate on developing processes.
Please contact your local Evatec sales & service organization to take the first step.

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