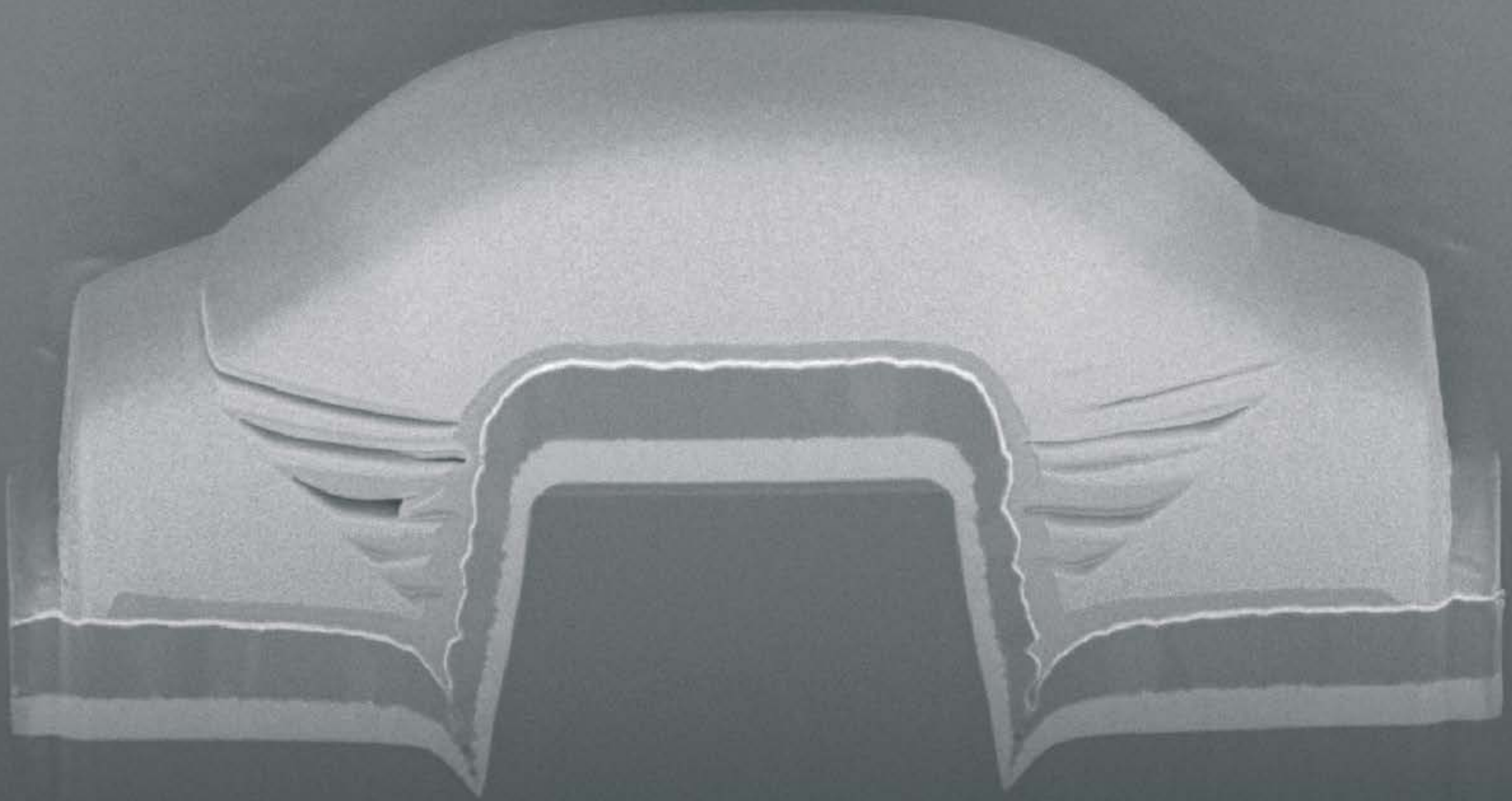
Side Wall coverage – maximizing performance in new generation optoelectronic devices

Head of Business Field Compound & Photonics, ***Jakob Bollhalder*** explains why device side wall coverage is becoming important for thin film processes in Optoelectronic applications like Micro LED and how Evatec thin film solutions on CLUSTERLINE® can deliver just the performance required.



It's all about maximizing device performance

As device architectures get smaller, the output area of the device front surface gets smaller too, and that means that any light losses from side walls which would normally not be critical for larger devices start to represent a bigger and bigger proportion of the overall light output. But there are other factors to consider too! As device architectures shrink to 50 microns and lower, so does device volume to surface area ratio. Protecting the device by effective side wall coverage becomes important to avoid device performance degradation and maximize lifetime.

Figure 1a: CLUSTERLINE® 200 equipped with single process modules and FOUP

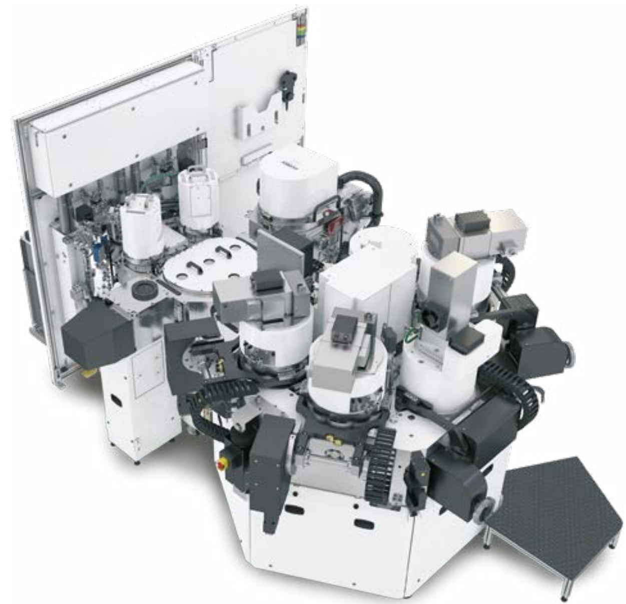


Figure 1b: CLUSTERLINE® 200 BPM equipped with Batch Process Module

CLUSTERLINE® 200 is the solution

Evatec's CLUSTERLINE® family is already a proven workhorse in the optoelectronics industry for applications including Micro LED, Mini LED and Edge-emitting Lasers (EELs). Processing of 200mm wafers either direct or on carriers makes it a flexible choice for sputter deposition of metals, TCOs, DBRs and passivation layers. Cassette-to-cassette configuration eliminates manual handling avoiding the risk of wafer breakage and reduces particles to the levels essential for high yield production of small scale devices. Different typical system layout for applications in optoelectonics are shown in Figure 1 for either single substrate or batch processing. Systems can be equipped with Advanced Process Control techniques like GSM broadband optical monitoring for layer termination and PEM plasma emission monitoring for control of film stoichiometry and maximizing deposition rates according to customer process. The systems are equipped with Evatec's proprietary cathode technology to deliver optimized side wall coverage.

Characterizing side wall coverage process performance

Every customer has their own unique device architectures and process requirements. Mapping performance of our tool and processes helps us be ready for whatever requests come our way. Figure 2 shows how we typically map side wall coverage performance on 8 inch substrates using a series of structures – pillars, trenches or vias of different dimensions.

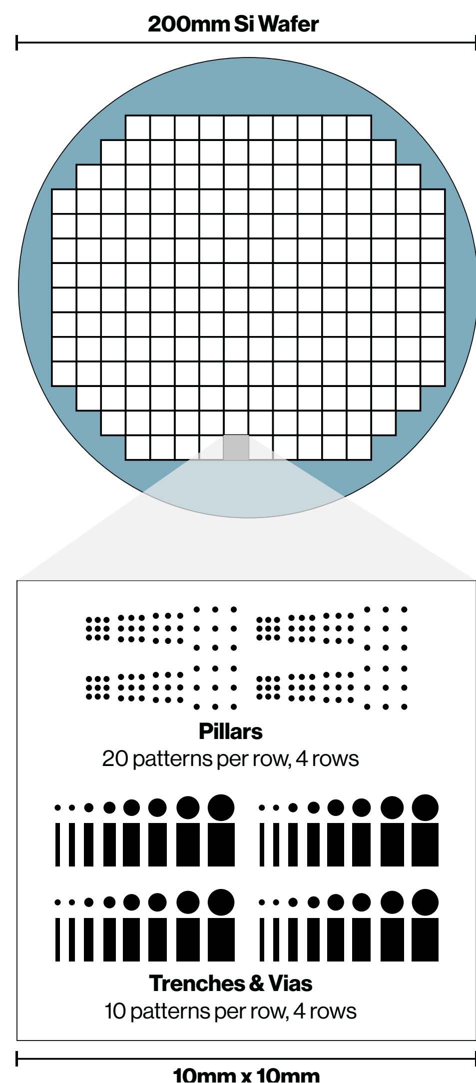


Figure 2: Side wall coverage performance test structures on wafer

Results so far

MicroLED technology

Figure 3a shows the architecture of a typical Micro LED while Figure 3b shows the excellent side wall coverage for ITO and metal layers when deposited on test structures using Evatec's propriety cathode technology.

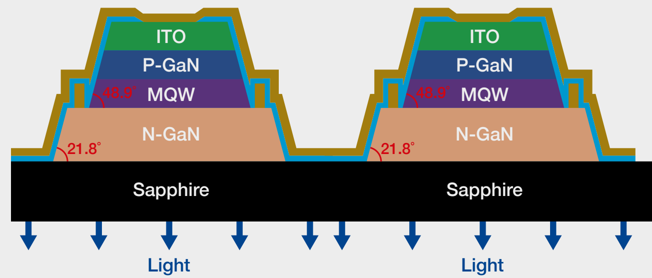


Figure 3a: Typical MicroLED architecture with side wall coverage for improved light extraction efficiency and passivation layer for device protection

EEL technology

MicroLED is just one area where innovations in coating processes for side wall coverage can be beneficial. New wafer level manufacturing approaches for edge emitting lasers eliminate the need for the processing of so called "laser bars" within complex mechanical jigs. Diode structures can be created within the wafer itself by lithography, etch and deposition stages and can then can have opposing facets (side walls) coated with the required high reflectivity (HR) or antireflection (AR) coatings whilst still at wafer level.

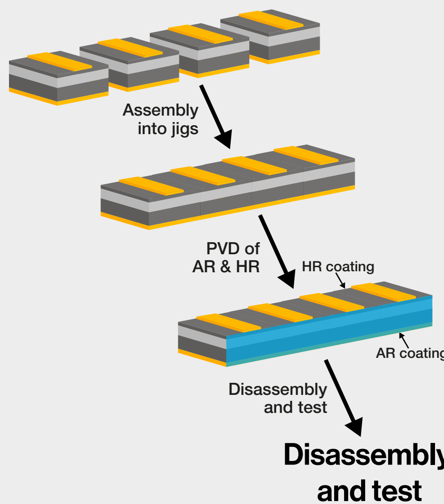
Figure 4 illustrates a typical process flow for EEL manufacturing according to two different manufacturing methods. In a traditional approach so called laser bars have to be assembled in a jig, coated on the first side then flipped and coated on the second side. In the Wafer Level Approach, photo-lithograph and etch steps are followed by coating steps to prepare devices over the whole wafer before final testing and dicing.

Traditional approach

*In a **traditional** approach so called laser bars have to be assembled in a jig, coated on the first side then flipped and coated on the second side.*

Wafer level approach

*In the **Wafer Level** approach coating technology for effective side wall coverage enables elimination of complex tooling and reduces overall process complexity.*



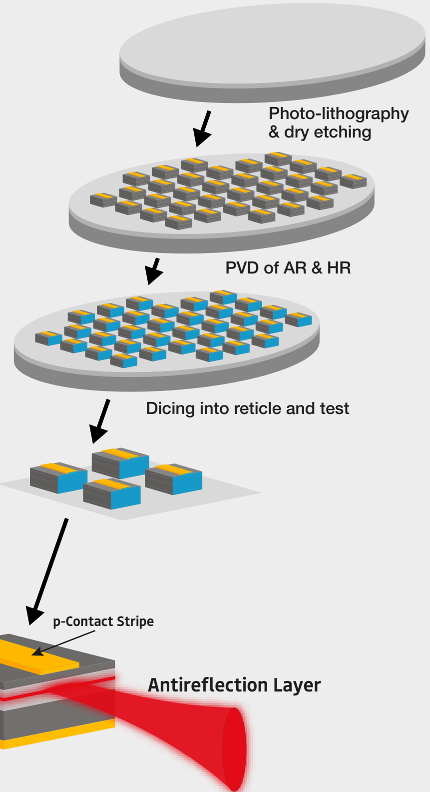


Figure 4: Typical process flow for EEL manufacturing

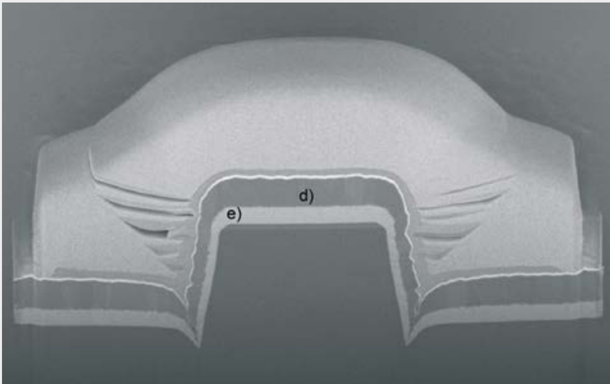
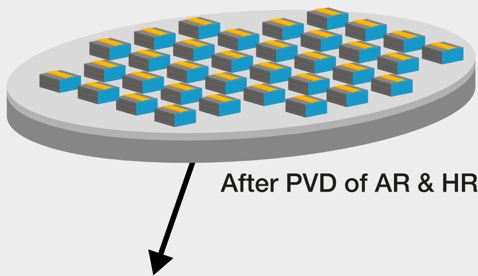
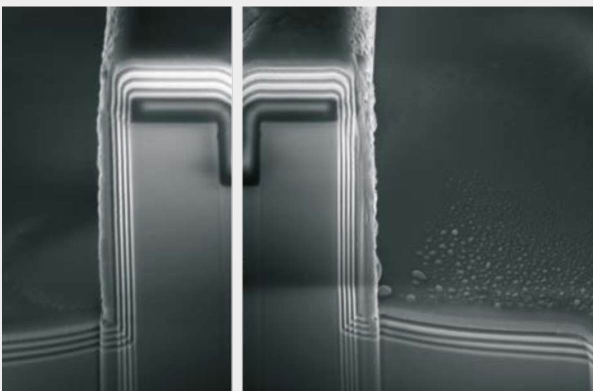


Figure 3b: Test structure deposition – d) Evatec Al; e) Evatec ITO





- Same result for both active sides
- Clear and smooth layer separation
- Equal single layer thickness on side wall
- Side wall coverage 60% of top thickness

Want to know more?

Our applications team would love to talk to you about the work we have been doing and find out how new approaches can support your own efforts in driving down manufacturing costs or improving process performance.

Contact us via your local Evatec sales and service office for more information
https://evatecnet.com/about-us/sales-service/

CLUSTERLINE® Family

CLUSTERLINE® 200 BPM