SCALING TO FINE FEATURES FOR CHIPLETS ON LARGE PANELS

Tim Olson, Founder & CEO of Deca and Evatec's **Roland Rettenmeier,** Senior Product Marketing Manager, Business Unit Advanced Packaging, explain the history, development and benefits of M-Series™ and Adaptive patterning and how roll out of volume manufacturing by industry leaders including Nepes and ASE demonstrates that the technology has a bright future.

Deca was born out of a passion to transform the way the world builds advanced electronic devices. In our first decade, our 10X thinking brought to life exciting breakthroughs including M-Series™ fan-out wafer level packaging (FO-WLP) and Adaptive Patterning™. Through divestiture of manufacturing operations in 2020, Deca became a pure-play technology and licensing company.

From the earliest days, the influence of SunPower's large format solar wafer manufacturing process underpinned Deca's vision of creating the highest levels of electronic interconnect technology on a large panel format. FO-WLP provided the physical realization through M-Series and Adaptive Patterning, now shipping in high volume and found in the world's leading Smartphones facilitated by emerging industry standards. The strong market growth figures expected for the FO Panel market up until 2023 are illustrated in figure 1.

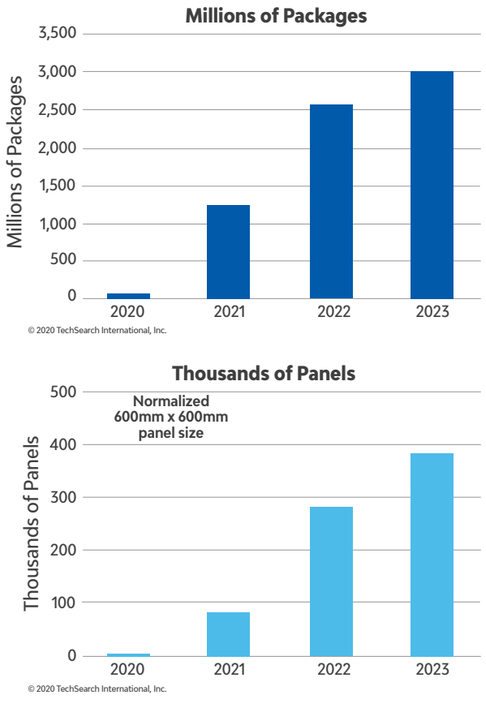


Figure 1: Forecast for low-density FO Panel Demand. Courtesy of Tech Search.

Multiple industry analyst reports, including the i-micronews article published in July 2019[1] have outlined the quality and reliability benefits of M-Series which sets the technology apart from industry competitors. M-Series is a chips-up fan-out technology. Cross-sectional views of chips-down fan-out (eWLB) and TSMC's chips-up fan-out (InFO) are shown in figures 2 and 4 respectively with M-Series in figure 3.

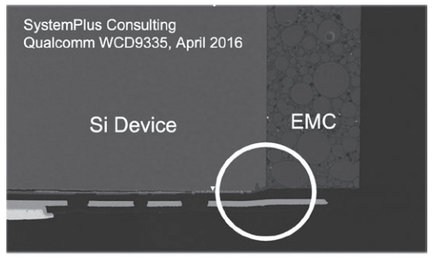


Figure 2: eWLB.

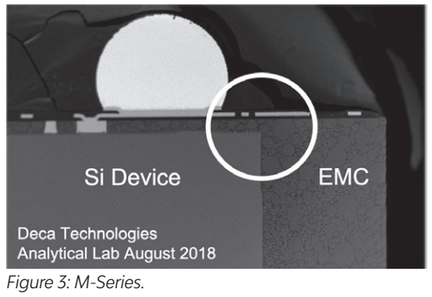


Figure 3: M-Series.

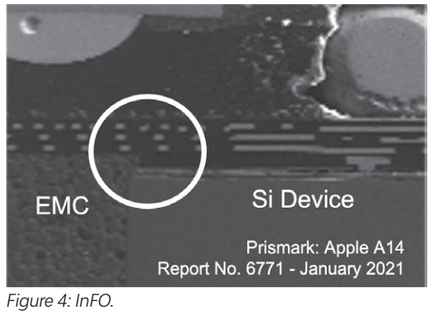


Figure 4: InFO.

Conventional fan-out is manufactured in a face-down process flow with the active face of the semiconductor device left exposed after the molding step. As encircled in figure 2, there is a discontinuity between the device surface and the electronic molding compound (EMC) leading to multiple process limitations as well as quality and reliability concerns. As highlighted in figure 3, the M-Series structure embeds the sensitive active semiconductor region of the device within EMC while providing a planar surface to alleviate process concerns in subsequent fab build-up layer processing. The embedded nature of M-Series with the EMC buffer layer over the device has been proven to significantly extend BLR (board level reliability) as compared to conventional WLCSP (wafer level chip-scale packaging) and eWLB which rely only on a polyimide (PI) or polybenzoxazole (PBO) material over the semiconductor device. While not easily discernable, the InFO structure shown in figure 4 similarly provides a planar surface for fab build-up layer processing, however, still relies on PI or PBO as the only protective material between the device and the electronic appliance printed circuit board (PCB).

Deca has established technology and license agreements with ASE Group (Advanced Semiconductor Engineering Inc.), the world's largest outsourced semiconductor assembly and test company (OSAT), and Nepes Corporation, a leading-edge provider of wafer and panel-level packaging foundry turnkey solutions. M-Series is currently produced in volumes measured in millions per day on 300mm wafer formats with plans in progress for full 600mm implementations at both Nepes and ASE to support robust demand growth. Multiple other manufacturing service providers including wafer foundries, substrate producers, and OSATs are in technology and licensing discussions or under consideration for expansion of the global M-Series and Adaptive Patterning production footprint.

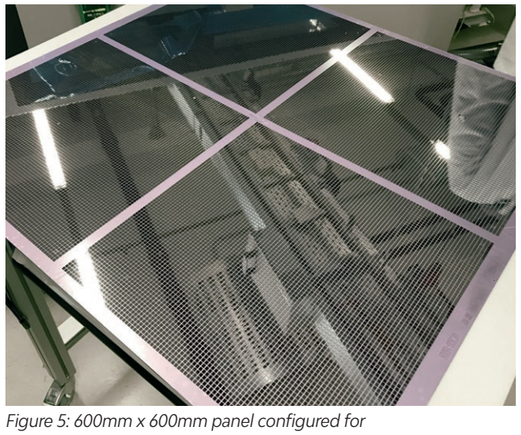


Figure 5: 600mm x 600mm panel configured for quartering to 300mm square panels.

Deca established the new 600mm x 600mm large panel manufacturing format for M-Series in 2010 with considerations for both short-term implementation and long-term optimized productivity.

The ability to segment the 600mm format into four equal 300mm square sub-panels as illustrated in figure 5 for use with conventional 300mm round wafer probe test equipment was a key short term consideration. 300mm square segments also provided achievable initial process extension targets for uniformity on critical processes including metal deposition, thin film coating and direct-write lithography while keeping in mind the ultimate utilization goal of the entire 600mm panel area. Seed layer deposition is one of the most critical process steps in manufacturing vertical and horizontal interconnects and has a direct impact on the overall package reliability and performance.

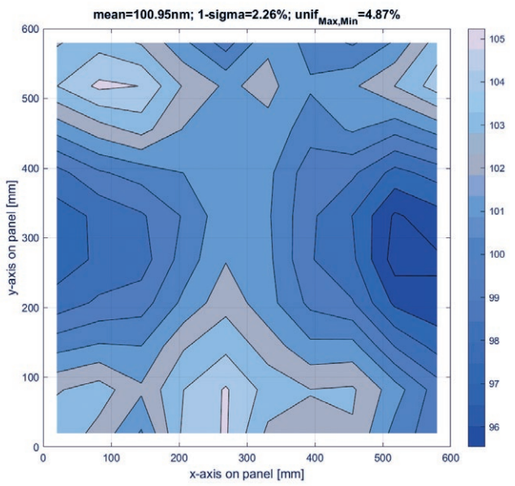


Figure 6a / 6b: Deposition uniformities on 600mm panels processed on CLUSTERLINE® 600 courtesy of Evatec.

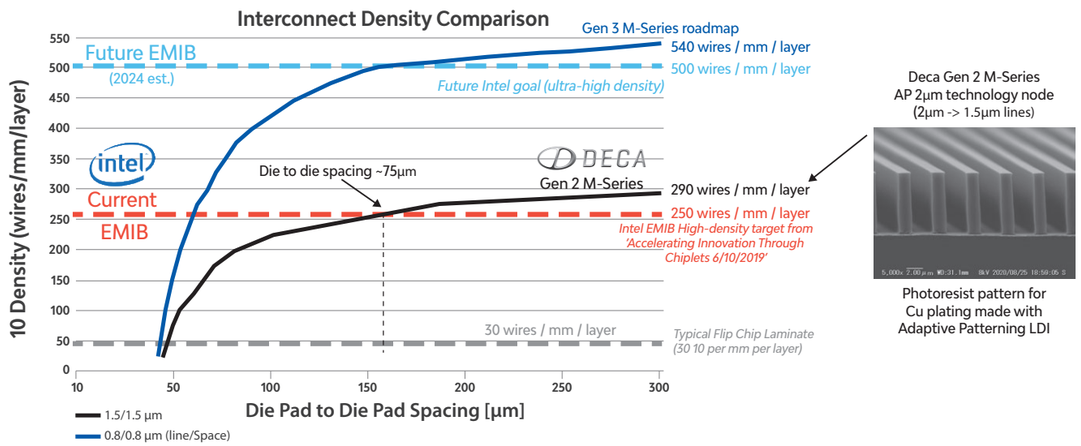
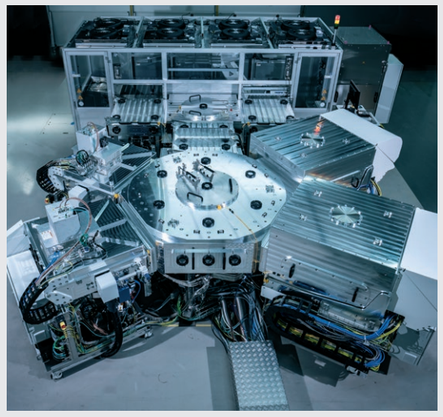


Figure 7: Wiring density comparison of EMIB vs. Gen 2 M-Series.

Successful 600mm panel processing calls for high performance degas, etch and sputter deposition processes across the full substrate area, plus well managed substrate temperature throughout the whole process to ensure low contact resistance (Rc) and excellent adhesion of the deposited seed layers prior to downstream electroplating and lithography processes. Figures 6a and 6b show that deposition uniformities for Ti and Cu layers deposited on commercially available production tools like Evatec's CLUSTERLINE® 600 now fall well within required specifcations.

In scaling up to the 600mm format, provisions for scaling down to 2µm line and space have also been included. One of the most critical capabilities supporting the simultaneous scaling up in panel size and down in feature size is Adaptive Patterning which introduces real-time design during manufacturing to accommodate natural process variation. Adaptive Patterning includes Deca's proprietary AP Studio EDA tool where designers create rules and boundaries within a new product design that are executed upon for each device in every wafer (or panel) within AP Engine performing real-time design during manufacturing. Through mask-less laser direct imaging (LDI), a unique design file for every device is utilized to align, re-route or re-shape any or all dielectric and metal build-up layers in real-time to ensure precise creation of the as-built semiconductor interconnect. With the latest 2µm line and space capability, benchmark high-density interconnect of over 200 wires/mm/layer can be achieved together with 20µm area array bond pad pitch. For heterogeneous integration of chiplets, these capabilities provide competitive, and in some cases, superior, capability to industry leading solutions including Intel's EMIB (embedded multi-die interconnect bridge) and TSMC's InFO (integrated fan-out).

Deca's Gen 2 M-Series and Adaptive Patterning technology achieve equivalent wiring density as compared with Intel's EMIB as shown in figure 7.



CLUSTERLINE® 600

"Evatec's CLUSTERLINE® 600 is qualified at major OSAT and IC-Substrate maker for superior degassing, etching and seed layer deposition - one important piece of the whole puzzle.

We are looking forward to see Deca's technology lift off and boost FOWLP and FOPLP to the next level. Smaller L/S geometries and smaller pads sizes for more precise vertical interconnects and more space for routing offer big potential to the packaging industry."

Roland Rettenmeier,
Evatec

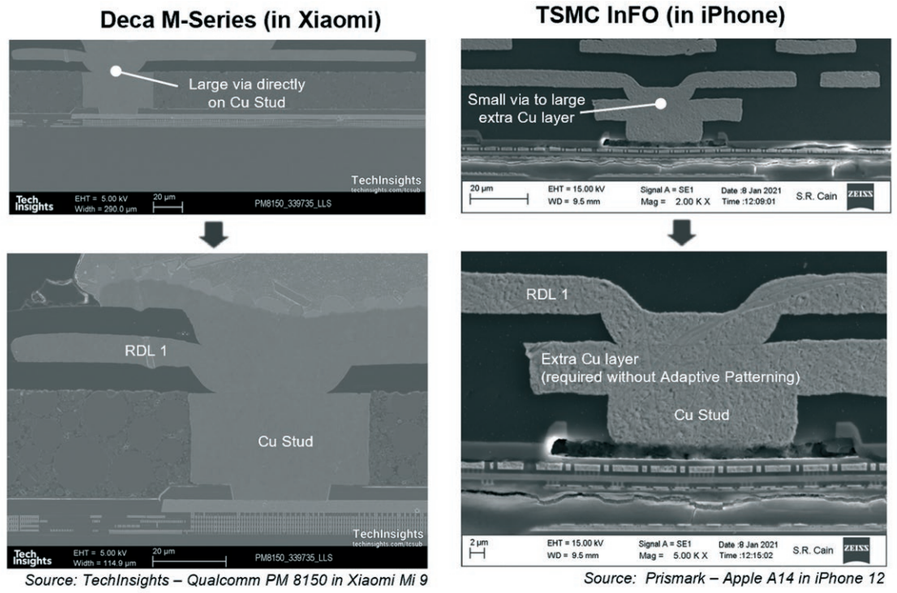


Figure 8: Device bond pad interface critical dimension comparison.

Source: TechInsights – Qualcomm PM 8150 in Xiaomi Mi 9

Source: Prismark – Apple A14 in iPhone 12

M-Series achieves equivalent density to the bridge chip structure within a simple planar fan-out RDL build-up eliminating the cost and complexity of embedding silicon bridge chips within a substrate.

Through the use of Adaptive Patterning, M-Series provides the capability to scale bond pad pitches to ever finer levels. Generation 1 provides the ability to scale to 45 µm area array bond pad pitch with a robust 15 µm polymer via precisely alignment to a 30µm Cu stud while Gen 2 supports a breakthrough 20µm array bond pad pitch using a 6µm polymer via precisely aligning to a 12 µm Cu stud, In comparison, TSMC's latest InFO is restricted to broader bond pad pitches with an oversized 50µm extra Cu layer added above the Cu stud to compensate for the lack of Adaptive Patterning. Third party teardown analyses showing Deca's Gen 1 M-Series vs. TSMC's latest InFO found in the Apple iPhone 12 is shown in figure 8.

For this specific power management device, a larger 50 µm Cu stud was chosen by the customer along with a 30 µm via connection made through Adaptive Patterning directly to the Cu stud without the need for an extra Cu layer.

In summary, as the semiconductor industry transitions away from monolithic silicon scaling in favor of heterogeneous integration and chiplets, fan-out technology is increasingly becoming the preferred choice of IC designers and system architects. Deca's M-Series fan-out with Adaptive Patterning is positioned to grow from its current Gen 1 leadership position in single die applications to the plan of record for ultra-high-density chiplet integration with Gen 2. With ASE's and Nepes' four combined manufacturing facilities in three countries in production or preparing for qualification along with multiple other potential licensees coming soon, scaling to fine features for chiplets on large panels with M-Series and Adaptive Patterning is on a well-defined path to success.

For more information visit **www.thinkdeca.com**

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Ref 1: https://www.i-micronews.com/new-commercialization-of-deca-technologies-fan-out-technology

Data and materials for all figures in this article (except 1 & 6) have been kindly provided by the author.