Electronics Packaging - From Afterthought to Product Differentiator

Industry guru, **Steffen Kroehnert**, shares his thoughts on the Advanced Packaging Industry and the emerging opportunities for Foundaries, IDMs and Suppliers.

Electronics packaging is generally divided into three major areas, Traditional Packaging - also called standard or mainstream packaging, and sometimes even just "Others" -, Advanced Packaging and Emerging Packaging Technologies.

Traditional Packaging is everything with wire or ribbon bond interconnects on ceramic, metal lead frame or organic laminated substrates, and it is typically a single die packaged. Advanced Packaging starts with Flip Chip interconnects (bumps, micro-bumps, Cu-Pillars), mainly on organic laminated substrates and has been growing during the last decade more and more into Wafer Level Packaging (WLP), which is Fan-in packaging with thin film processed RDLs (Redistribution Layers), Fan-out packaging on Wafer and Panel Level (Chip First - RDL Last, or RDL First - Chip Last, Face-up and Face-down approach), so called 2.5D interposer technology with Thru Silicon Via (TSV) with passive or more recent also active interposer, 3D Packaging such as die stacking, package stacking with Thru Package Via (TPV, which can be pre-formed or post-formed and e.g. Thru Mold Via (TMV), or Thru Glass Via (TGV)), 3DIC with TSV (via first, via middle and via last concepts), System-in-Package (SiP), and many different combinations of those, which are summarized under the term Heterogeneous Integration.

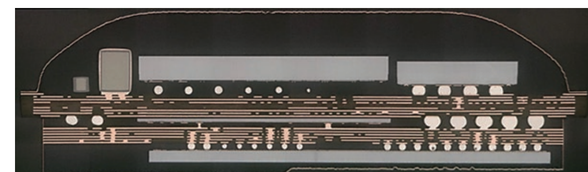
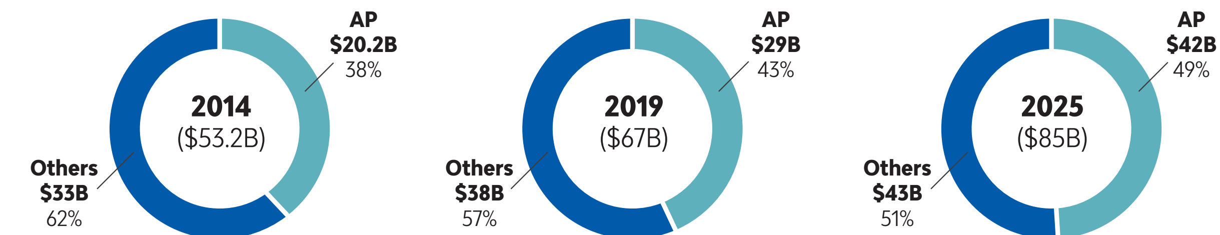


Figure 1: Highly Integrated 3D-SiP: Apple AirPods Pro SiP Cross-Section.

Under the title "**Heterogeneous Integration Roadmap (HIR)**: Driving Force and Enabling Technology for Systems of the Future", the executive summary of the roadmap talks about the vision of the HIR, which is available to everyone. "It became one of the most important roadmaps in the semiconductor world, after the International Technology Roadmap for Semiconductors (ITRS) was discontinued. The SIA7 (Semiconductor Industry Association) brought the ITRS to closure in July 2016, but we are now in a new world order with changes and disruptions that we could never have imagined before. The executive summary continues... "the need for roadmapping has never been clearer. The business landscape is experiencing great change with the continued rise of technology companies that are driving social media, cloud computing, search, online commerce, and big data, leading to integrated hardware-software driven applications and unprecedented growth of application spaces".

Looking at the Electronics Packaging market, we are seeing fast growth and new chances. The chances are not only for the typical players in this market, the OSAT, IDM and EMS companies, but also for Foundries and Material Suppliers stepping up in the value chain, and taking over an increasing share of the Advanced Packaging market. According to Yole Développement in France, the total packaging market is predicted to grow from \$53.2B in 2014 to \$85B in 2025. Advanced Packaging is going to count for 49% of that, coming from 38% in 2014. That is just an 11% higher share, but as the total packaging market is growing, the revenue in Advanced Packaging is predicted to more than double from \$20.2B in 2014 to \$42B in 2025. In 2019, wireless communication and consumer applications generated 85% of Advanced Packaging revenue.

Figure 2: Advanced Packaging Landscape in Post-COVID Economy - Live Market Briefing" Yole Développement, July 16, 2020.



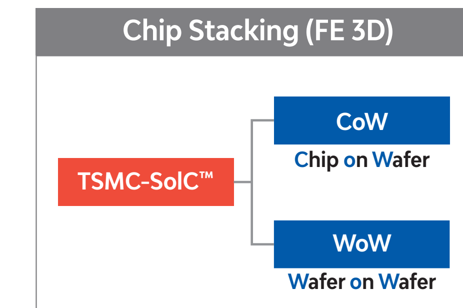
Also, the traditional packaging market revenues are going up by more than \$10B from \$33B in 2014 to \$43B in 2025. It is just its share in the total packaging market, which is growing as a whole, that is predicted to decrease by 11% from 62% in 2014 to 51% in 2025.

The COVID-19 pandemic impacted packaging revenues heavily. However, the revenue reductions of around 7% in 2020 are expected to be followed by a strong recovery in 2021 with around 14% growth. The traditional packaging market suffered more with a revenue drop of around 15% in 2020.

The main drivers for Advanced Packaging are the new mobile communication standard 5G, Artificial Intelligence (AI) and Deep Machine Learning combined with "Big Data" and High Performance Computing (HPC) in data centers, as well as the Internet of Things (IoT). Another driver bringing more value to Advanced Packaging is the fact that monolithic integration in System-on-Chip (SoC) slowed down and with it the realization of the so called "Moore's Law", an economic observation made by Gordon Moore, CEO and Co-Founder of Intel, in 1965. He prdicted the number of transistors in a dense Integrated Circuit (IC) was going to double every year for at least one decade, which he revised in 1975 to every two years. After "More Moore", the "More than Moore" technologies are increasingly required to continue "Moore's Law" at system integration level, and those are mainly Advanced Packaging technologies. That is also the main reason for Compound Annual Growth Rates (CAGR) 2019-2025 of 12.3% for Fan-out Wafer- and Panel Level Packaging (WLP/PLP), 5.9% for Flip Chip, 1.3% for Fan-in WLP, 25% for 3D Stacking (includes portion of wafers not included in Flip Chip or Fan-in WLP as used for pre and/or postprocessing around the 3D Stacking), and 17% for Embedded Die.

In terms of processed wafers, the largest portion in the Advanced Packaging market (2019 vs. 2025) is still Flip Chip (75% vs. 71%), followed by Fan-in WLP (12% vs. 9%), 3D Stacking (7% vs. 12%), and Fan-out WLP/PLP (6% vs. 8%). Despite the impressive CAGR of Embedded Die stated before, its share in the Advanced Packaging market stays below 1% as the total number of processed wafers is growing in this time frame with a CAGR of 7% (29M vs. 43M).

TSMC is showing in their "3D Fabric" concept "Advanced Packaging (BE 3D)" technologies as InFO (Integrated Fan-out), a Chip First approach with different options such as InFO-R and InFO-L, and CoWoS® (Chip-on-Wafer-on-Substrate), a Chip Last approach with different options such as CoWoS®-S, CoWoS®-R and CoWoS®-L.



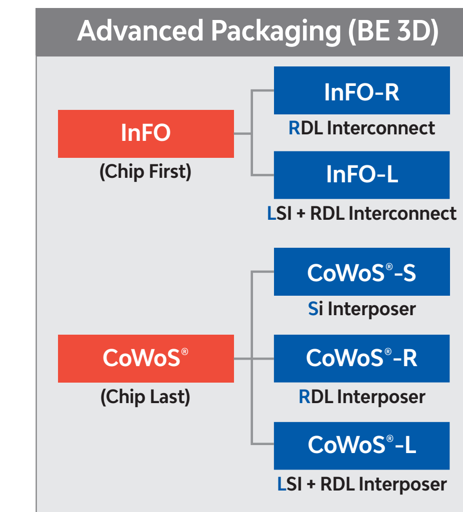


Figure 3: 3D Fabric™ Overview with FE 3D and BE 3D Solutions (Source: TSMC).

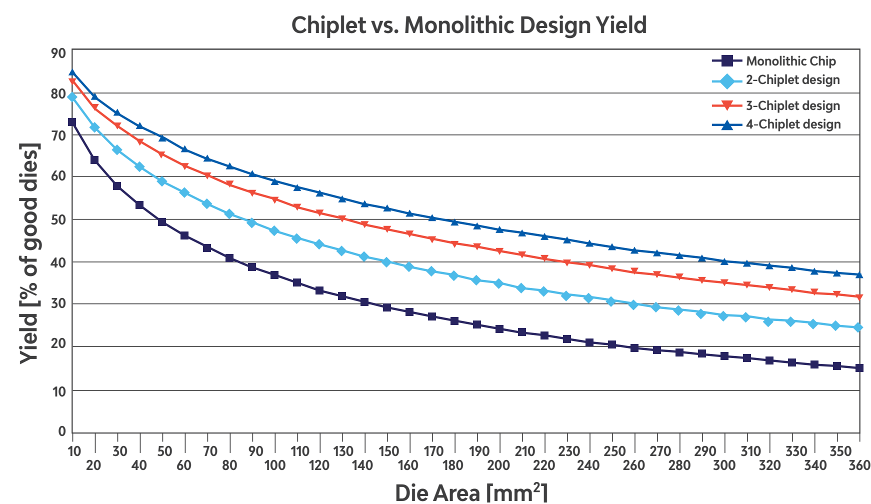


Figure 4: Wafer yield [%] in dependency on die size [mm²] on wafer (Source: WikiChip).

But wait, wouldn't we expect the names of the large OSAT companies like ASE Group, Amkor Technology, JCET Group, PTI, Tongfu Microelectronic or Tianshui Huatian Microelectronics here? TSMC is a Foundry, and that they are strongly involved in Advanced Packaging is underlining a trend when it comes to WLP. More IDMs and many Foundries are entering into that business taking a share from the OSATs. The reason is easy to understand. Advanced packaging technologies are getting closer to wafer fab processes, using wafer fab equipment, require clean room classes as used in wafer fabs due to the smaller features sizes such as RDL line width, spacing and thickness, via sizes and height, and contact pad pitches. The package is becoming a functional part of the product, chip-package-board co-design and co-development is essential, CPI (chip-package-interaction) considerations are crucial elements.

Looking at the revenues coming from its packaging business, TSMC would be the 4th largest OSAT in the world with an Advanced Packaging revenue of $2.88B in 2019, and business is continuing to grow. Back in June 2020, TSMC announced plans to invest $10.1B in building a new chip packaging and testing facility in Miaoli, northern Taiwan. The completion of the plant is scheduled for May 2021 with operations set to start mid of 2021.

Emerging packaging technologies are D2W (Die-to-Wafer) bonding and W2W (Wafer-to-Wafer) bonding with interconnects formed by TCB (thermo-compression bonding) or hybrid bonding, typically Cu pad to Cu pad without extra interconnect elements. TSMC is calling this in their "3D Fabric" concept "Chip Stacking (FE 3D)" SoIC™ (System-on-Integrated Circuit) with CoW (Chip on Wafer) and WoW (Wafer-on Wafer). This recently became a push from the need to disintegrate (de-integrate and break down a large chip into smaller parts) of large monolithic SoC (System-on-Chip) manufactured with latest wafer fab technology nodes such as 14 nm and below driven by the digital design into so called Chiplets/Dielets. Those are integrated functional circuit blocks, often reusable IP blocks, that have been specifically designed to work with other similar Chiplets to form larger more complex chips inside a SiP. They have been "invented" in the process of disintegration of SoC into many smaller chips for the following two main reasons:

- Process technologies continued to enable higher monolithic integration in one chip, but SoC sizes reached reticle limits, which dictated the maximum size of chip.
- Economics has resulted in a reversal of that trend due to defect density on large chips directly impacting yield and cost (Figure 4) and significant increased cost for new technology nodes.

Advanced Packaging got the task to enable the rebuilding of the large SoC out of those Chiplets/Dielets targeting the performance of the monolithic SoC or even better, as the functional blocks put together here are manufactured with function optimized wafer fab technologies in different companies with different capabilities, IP ownership, and consequently function specific optimized

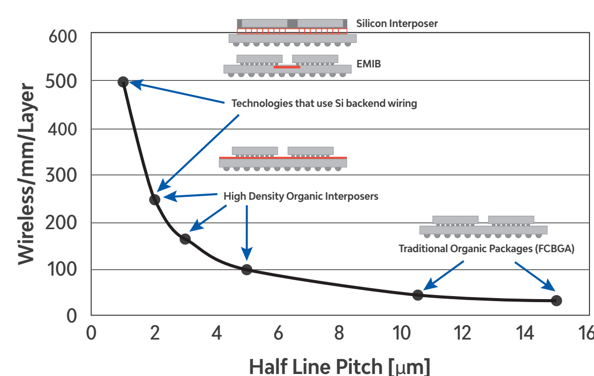
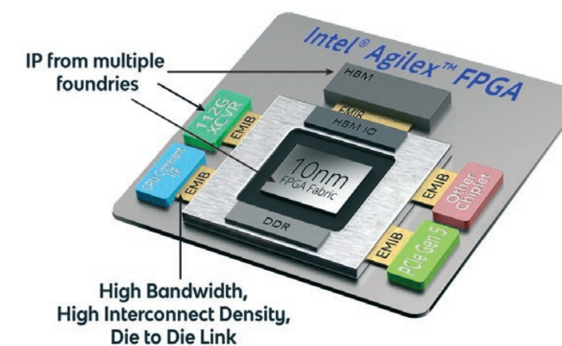


Figure 5: Interconnect density envelopes for different advanced package architectures (Source: Intel).

Figure 6: The Intel Agilex FPGA provides a good example of heterogeneous integration in SiP (Source: Intel).



performance. Customers can do a "Cherry Picking" to build their own "SoCs" out of the Chiplets they consider the best for their applications. However, there is still a lot of work to do such as standardization of interfaces, and development of smallest und shortest possible interconnection technologies between the Chiplets in the package, often thousands of contacts on a few square millimeters.

Given the trends summarized above and the growth in Advanced Packaging shown, the equipment supply chain will be under enormous pressure to support the technology development with tailored equipment and process solutions and to meet capacity and productivity requirements once the industry moves into high volume manufacturing.

A key piece of technology is thin film deposition, both on wafer and panel level up to 600mm square substrates.

Thin film deposition is required to manufacture either seed layers or passivation layers with high uniformity, superior adhesion, lowest resistance and low particle count. Innovative, flexible, high throughput, highly automated and high quality solutions are required by the packaging industry, which in this field are not only OSATs and IDMs anymore, but also Foundries as explained above. Last but not least, physical vapor deposition technology will make it into the Printed Circuit Board (PCB)/ IC-Substrate industry too, as technology leaders move towards smaller feature sizes too, competing with mainly the traditional Fan-out WLP/PLP players. Embedded trace and molded interconnect substrates e.g. using Ajinomoto build-up films (ABF) are on the rise and present new opportunities for thin film deposition technology leaders like Evatec.

About the author

Steffen Kroehnert is President & Founder of ESPAT-Consulting based in Dresden, Germany. He provides a wide range of consulting services around Semiconductor Packaging, Assembly and Test, mainly for customers in Europe. By June 2019, he had worked for more than 20 years in different R&D, engineering and management positions at large IDMs and OSATs in Germany and Portugal, namely Siemens Semiconductors, Infineon Technologies, Qimonda, NANIUM and Amkor Technology, where he most recently served as Senior Director Technology Development. Since 2016 Steffen has chaired the European SEMI integrated Packaging, Assembly and Test - Technology Community (ESiPAT-TC).

Steffen has authored or co-authored 23 patent filings and many technical papers in the field of Packaging Technology. He also co-edited the book "Advances in Embedded and Fan-out Wafer Level Packaging Technologies". He is an active member of several technical and conference committees of IEEE EPS, IMAPS and SEMI Europe. Steffen holds a M.Sc. in Electrical Engineering and Microsystems Technologies from the Technical University of Chemnitz, Germany.

Data and materials for all figures in this article have been kindly provided by the author.